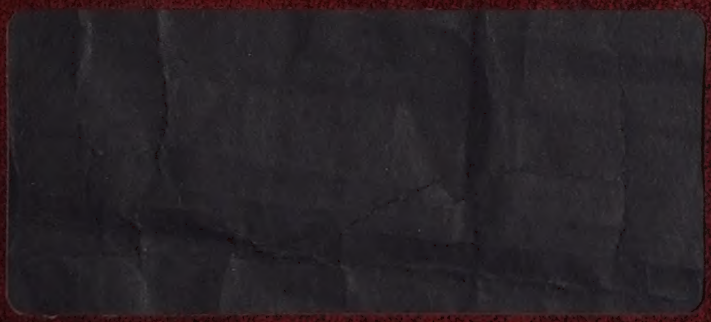
CAL LAB

Instruction manual



DATA I/O

ID# NC2980 S/N N/A

PAL
Program Card Set
909/919-1427

025-1427 REV G JAN 81

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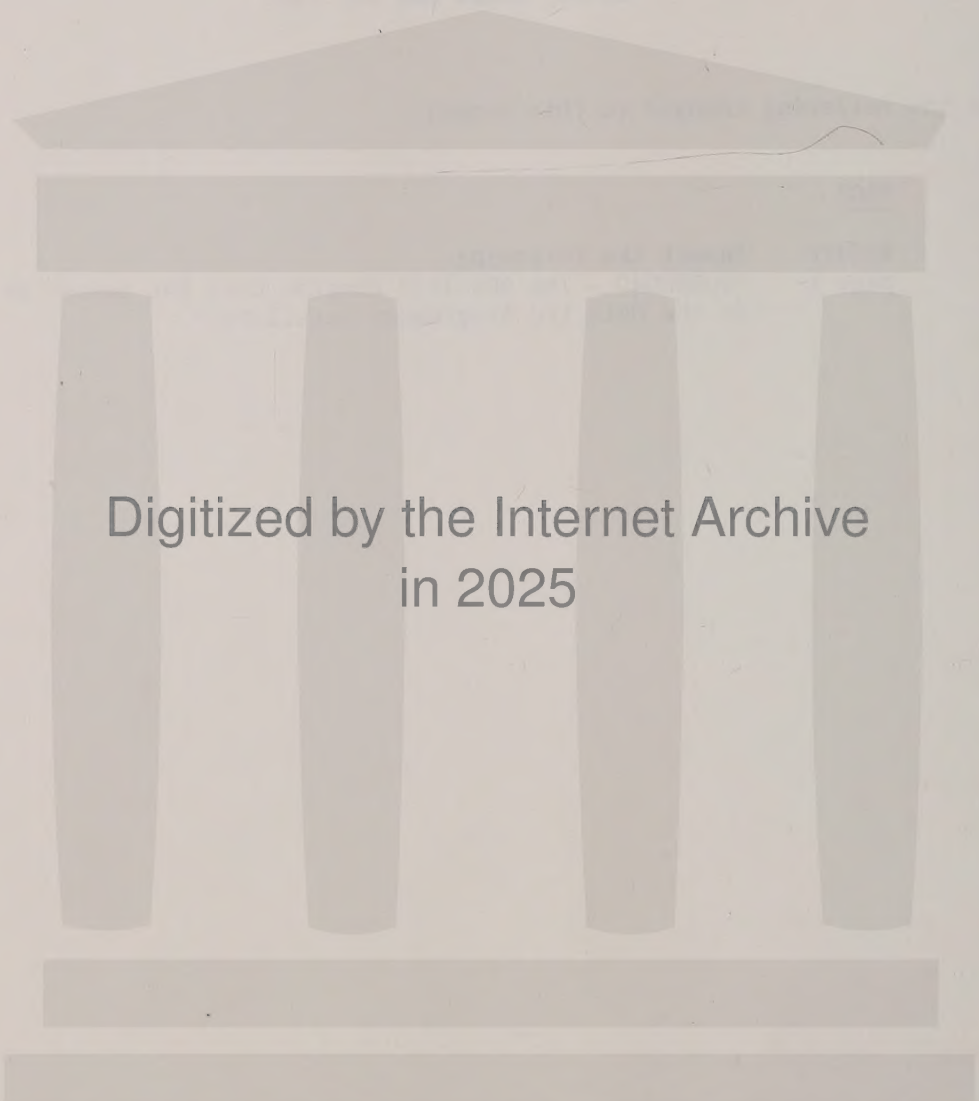
DATA I/O
PAL PROGRAM CARD SET MANUAL
025-1427 REV. R OR LATER

CHANGE SHEET MAY 29, 1980

Make the following changes to this manual:

NO.	PAGE	
1	Before page i	Insert the following: "FOREWORD - The 909-1427 Program Card Set cannot be used in the Data I/O Programmer Satellite."



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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size	PAL Part Number	Output	Pinout	Socket Adapter
MONOLITHIC MEMORIES				
10x8 FL	10H8	TS	20 PIN	1428-1
12x6 FL	12H6	TS	20 PIN	1428-1
14x4 FL	14H4	TS	20 PIN	1428-1
16x2 FL	16H2	TS	20 PIN	1428-1
10x8 FL	10L8	TS	20 PIN	1428-2
12x6 FL	12L6	TS	20 PIN	1428-2
14x4 FL	14L4	TS	20 PIN	1428-2
16x2 FL	16L2	TS	20 PIN	1428-2
16x4 FL	16A4	TS	20 PIN	1428-2
16x4 FL	16X4	TS	20 PIN	1428-2
16x4 FL	16R4	TS	20 PIN	1428-2
16x6 FL	16R6	TS	20 PIN	1428-2
16x8 FL	16L8	TS	20 PIN	1428-2
16x8 FL	16R8	TS	20 PIN	1428-2
16x2 FL	16C1	TS	20 PIN	1428-3

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).

1.2 CALIBRATOR PROGRAM ADAPTER

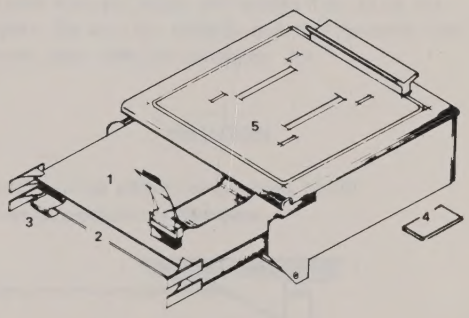
The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

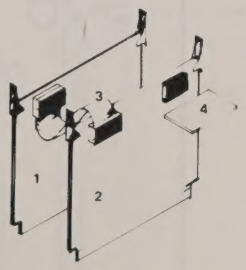
1.3 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1454
2. ANALOG CARD	701-1427
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1427
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer - Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP8	Reject	C	
JP11	Word Limit	512	Selection defaults to socket adapter

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

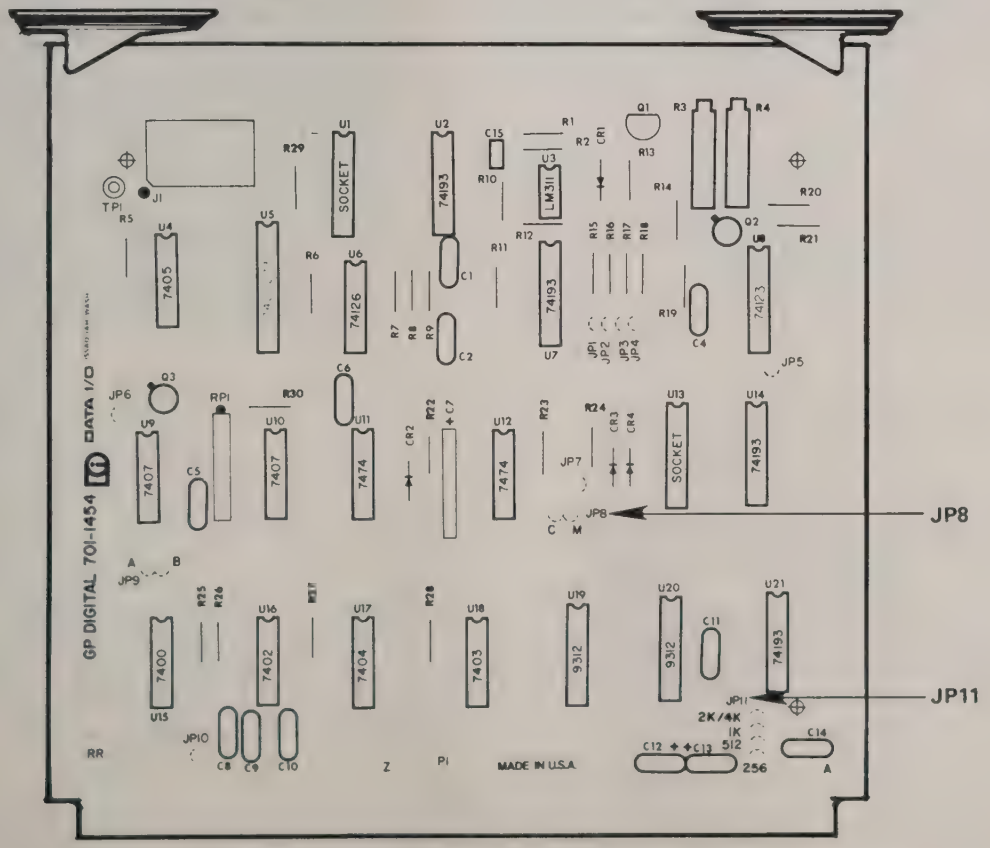


Figure 2-1. Digital Card Jumper Locations

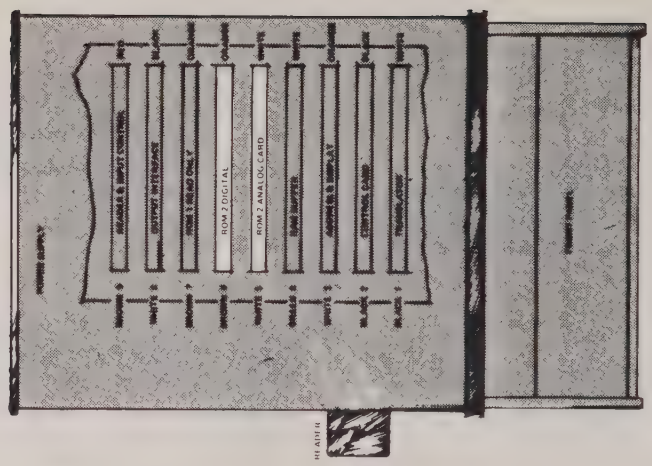


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

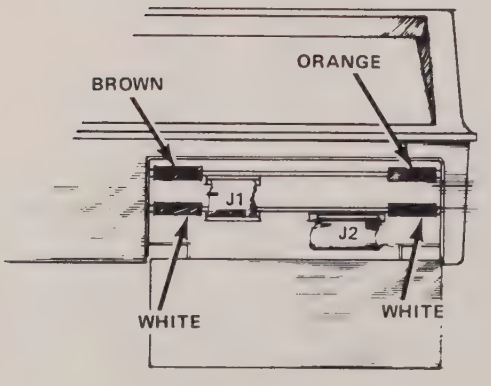


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

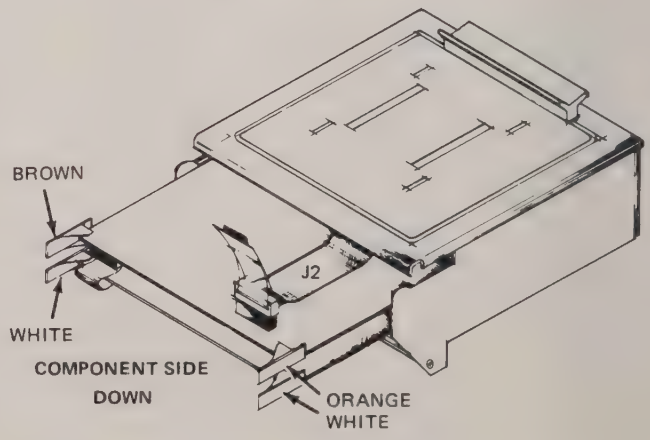


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

3.1 INTRODUCTION

There are fifteen Series 20 PALs, each in a 20-pin Skinny DIP package. All are programmable using the Data I/O 909/919-1427 Program Card Set and the appropriate socket adapter listed in Table 1-1.

PALs are like PROMs in that they have one fixed array and one array of fusible links. A PROM is a fixed AND array driving a programmable OR array; a PAL is a programmable AND array driving a fixed OR array. Some PALs in the Series 20 family have additional options, including:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

3.2 PROGRAMMING CONSIDERATIONS

To the Data I/O programmer, the PAL is configured as a 512x4 PROM. A fully populated PAL has 2048 fuses.

Not all PALs are fully populated; some have as few as 320 fuses. In programming any PAL, it is necessary to load programmer RAM with data for all 2048 bits. RAM locations corresponding to unpopulated PAL locations (where there are no fuses) must be loaded correctly in order for the programmer to verify all 2048 bits. The fuse-population patterns for the various PALs are given in the MMI *PAL Handbook.*

The last fuse in each PAL is reserved for protection of proprietary designs. If blown, this fuse prevents verification of the PAL. To reduce the possiblity of inadvertently making the PAL unreadable, blowing the last fuse requires a simple fixture, made according to the specification published by MMI.

3.3 PROGRAMMING THE PAL

Once the correct PAL has been chosen for a task and the desired logic functions have been specified, the next step is to organize a truth table to program into the PAL. Program data for blown fuses must be 1's and for fuses intact, 0's.

MMI PALASM program may be used to generate a truth table directly from logic equations. (See the *PAL Handbook.)* Alternately, a truth table may be prepared from a PAL Logic Diagram, Figure 3-1, using the PAL Programming Format Table, Figure 3-2.

When using keyboard data entry to the table, it is not necessary to hand-load the pattern of unpopulated locations. A simple method is to load RAM first from a virgin PAL of the same configuration as the one to be programmed. In this way the pattern of unpopulated locations is recorded in RAM; all that remains is to edit the data to selectively program fuses.

3.4 PAL PROGRAMMING FORMAT

The PAL Programming Format is designed to aid in organizing "state-of-the-fuse" information for truth table data entry into the programmer.

The vertical columns on the format table correspond to the horizontal lines on the logic diagram; these lines are the PAL Product Lines. The horizontal rows on the table correspond to the PAL Inputs, the vertical lines on the logic diagram.

Each horizontal row of four programmer bits is designated by a word count, or programmer RAM address. When using a programmer with a hexadecimal keypad, such as the System 19, each of these four-bit words must be converted to a hexadecimal digit. This digit is then entered into the corresponding RAM address.

Programmers with a binary keypad, such as the Model 5B, only require that the corresponding bits be entered into RAM at each address.

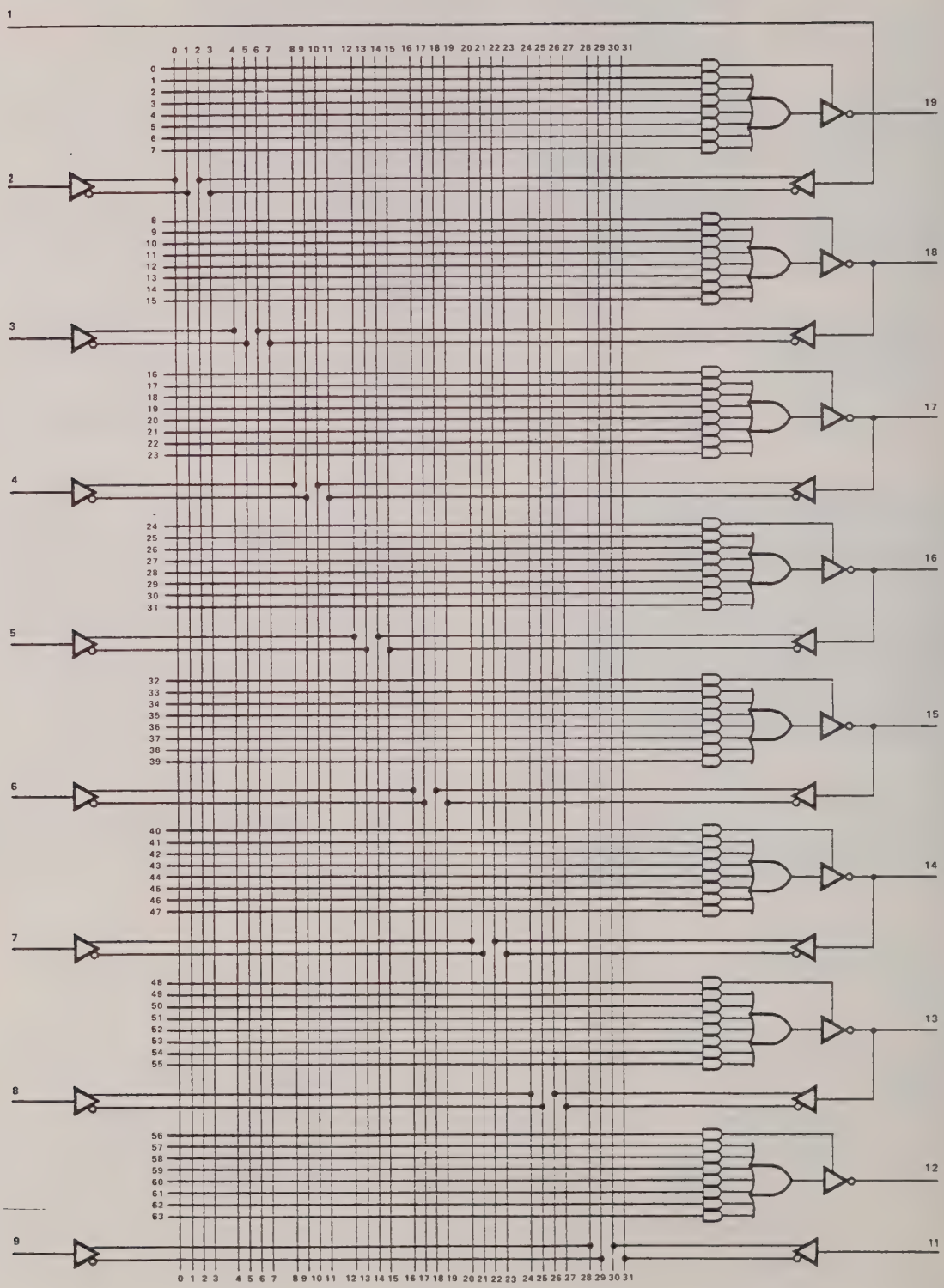
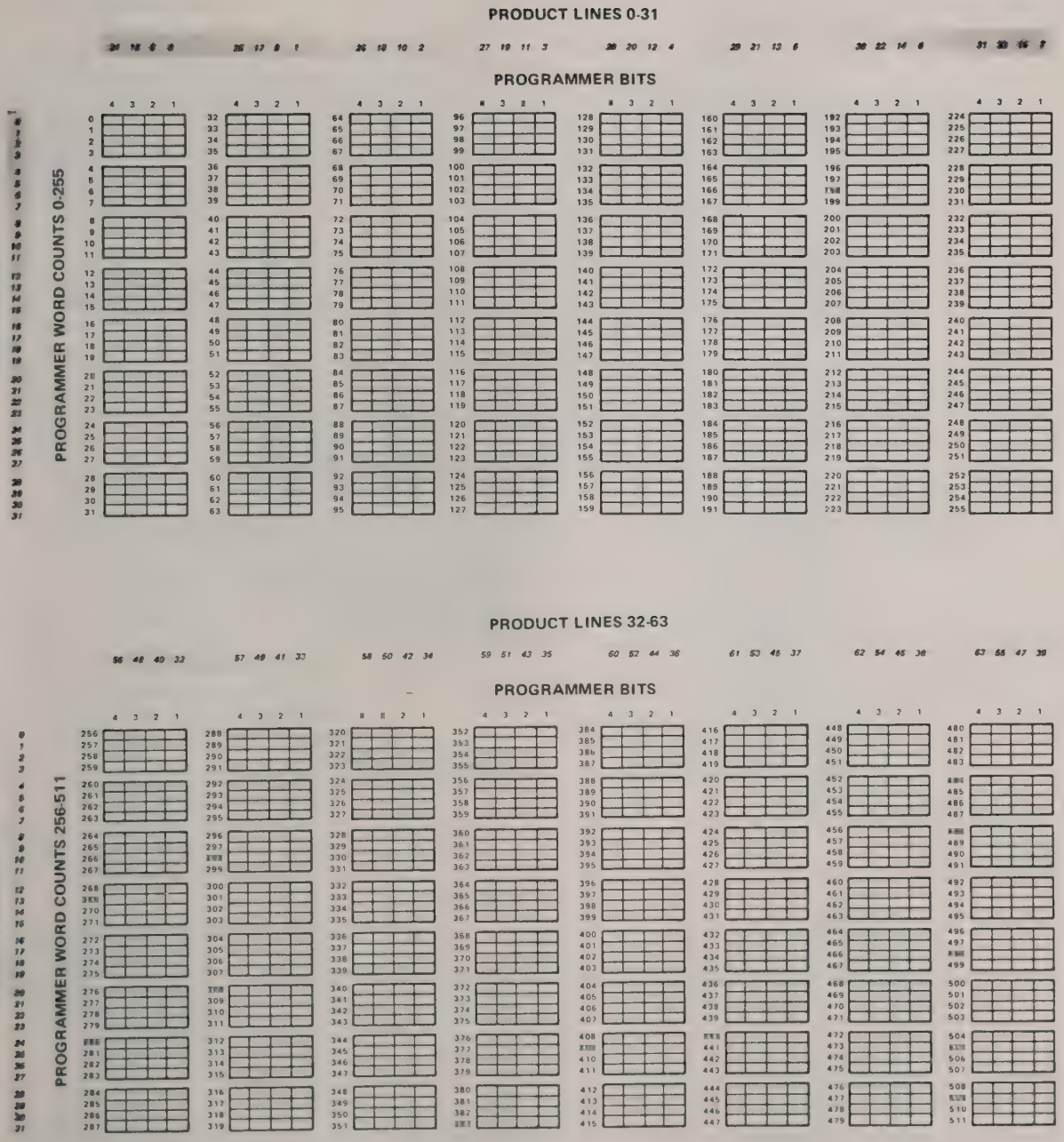


Figure 3-1. Example Logic Diagram (for PAL 16L8)



NOTES

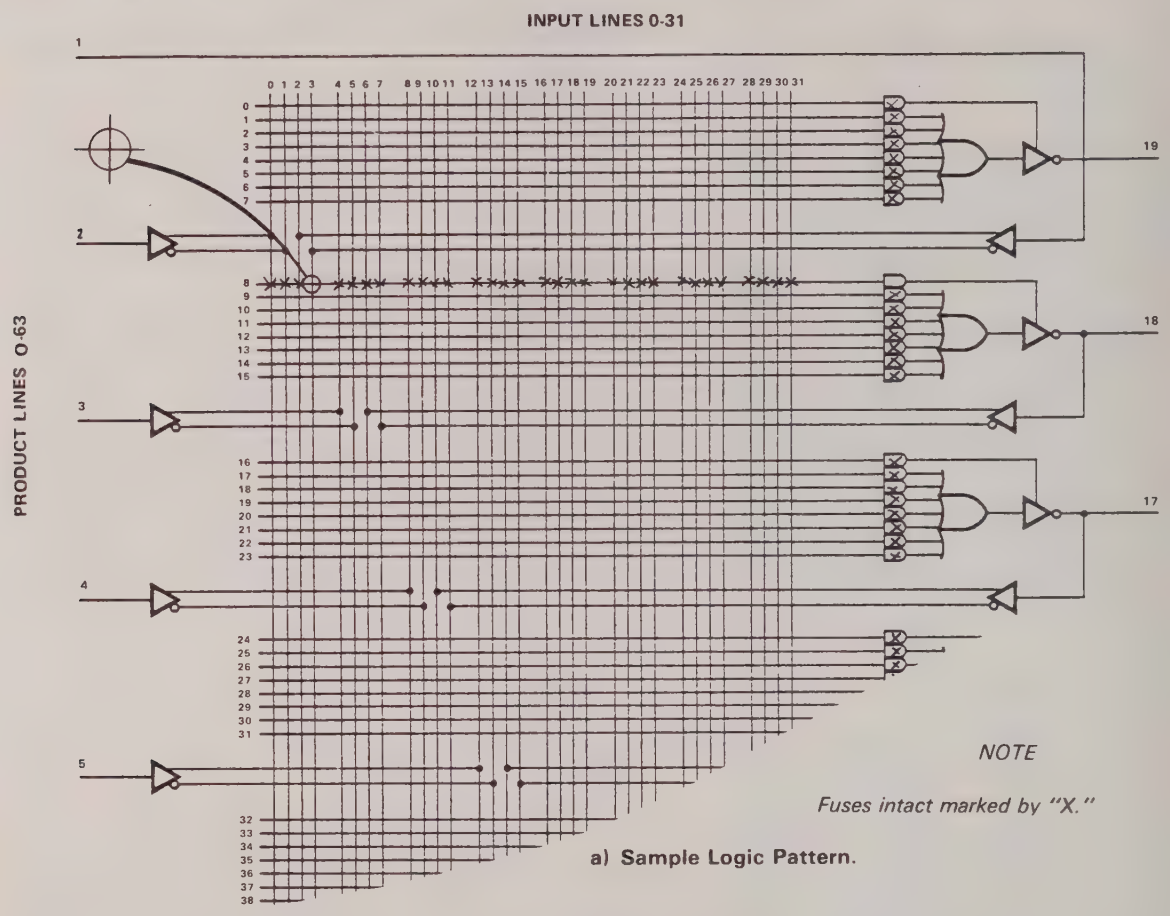
Numbers in italics refer to PAL lines on the PAL Logic Diagram. Numbers in block type refer to programmer RAM locations.

Figure 3-2. PAL Programming Format Table

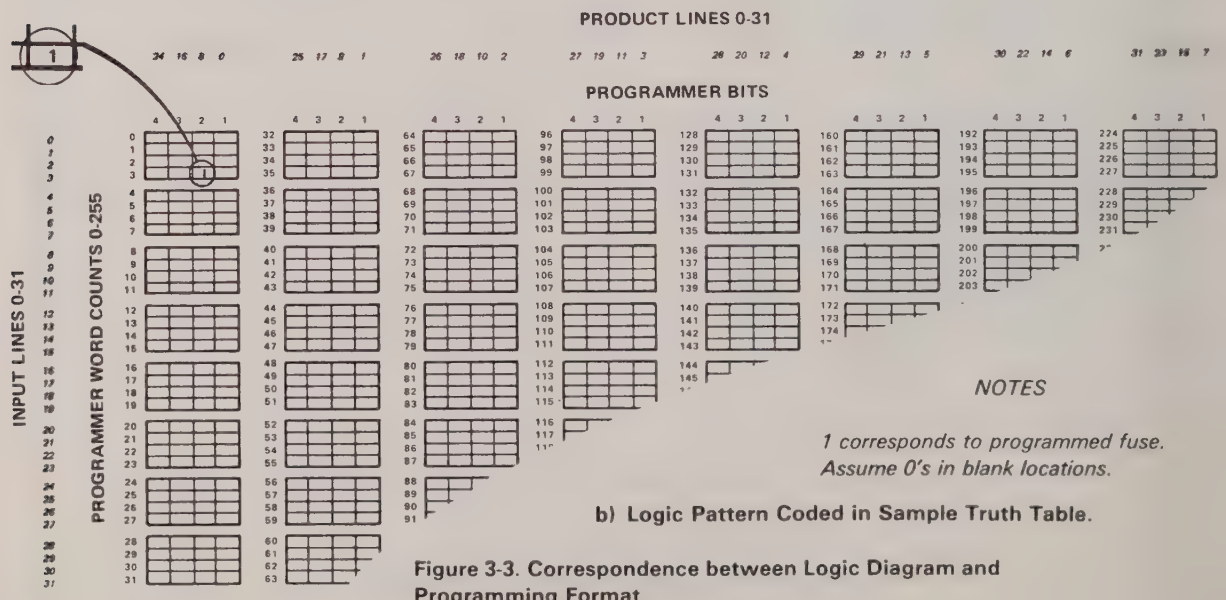
3.5 PAL DATA PROGRAMMING EXAMPLE

Figure 3-3 shows the transference of a single bit of data from the PAL Logic Diagram to the PAL Programming Format. According to MMI's symbol convention, an X on the Logic Diagram represents an intact fuse, and an unmarked fuse is programmed (blown). An X at the right end of a product line indicates that all fuses on that line are intact.

In the example, input 3 of product line 8 is the fuse selected when the programmer is at word count 3. Note that bit number 2 is used to program the fuse.



a) Sample Logic Pattern.



b) Logic Pattern Coded in Sample Truth Table.

Figure 3-3. Correspondence between Logic Diagram and Programming Format

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

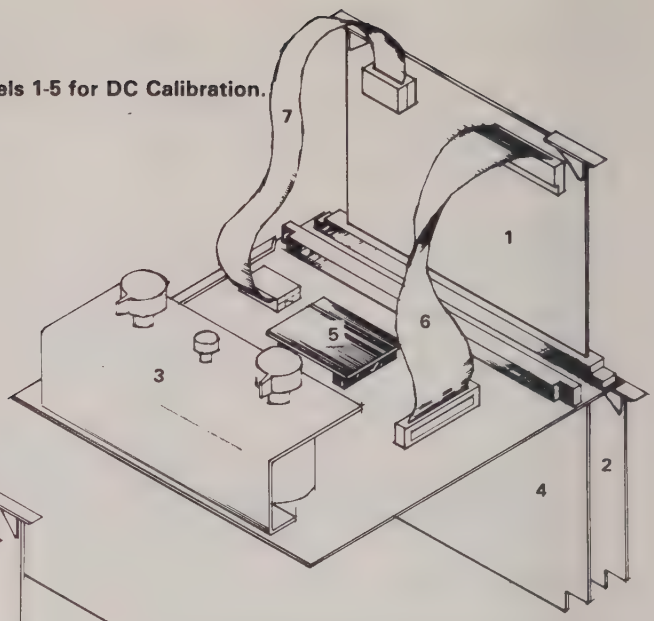
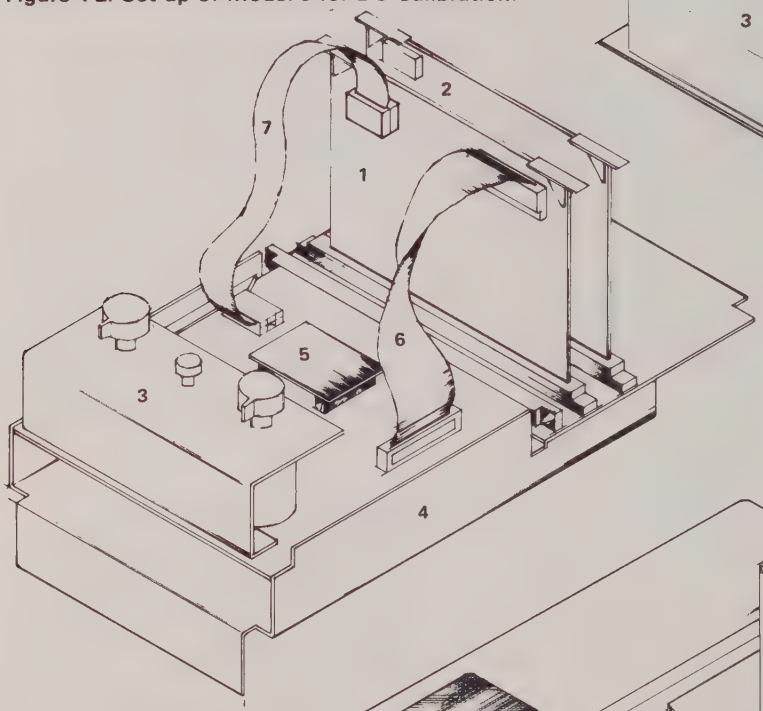
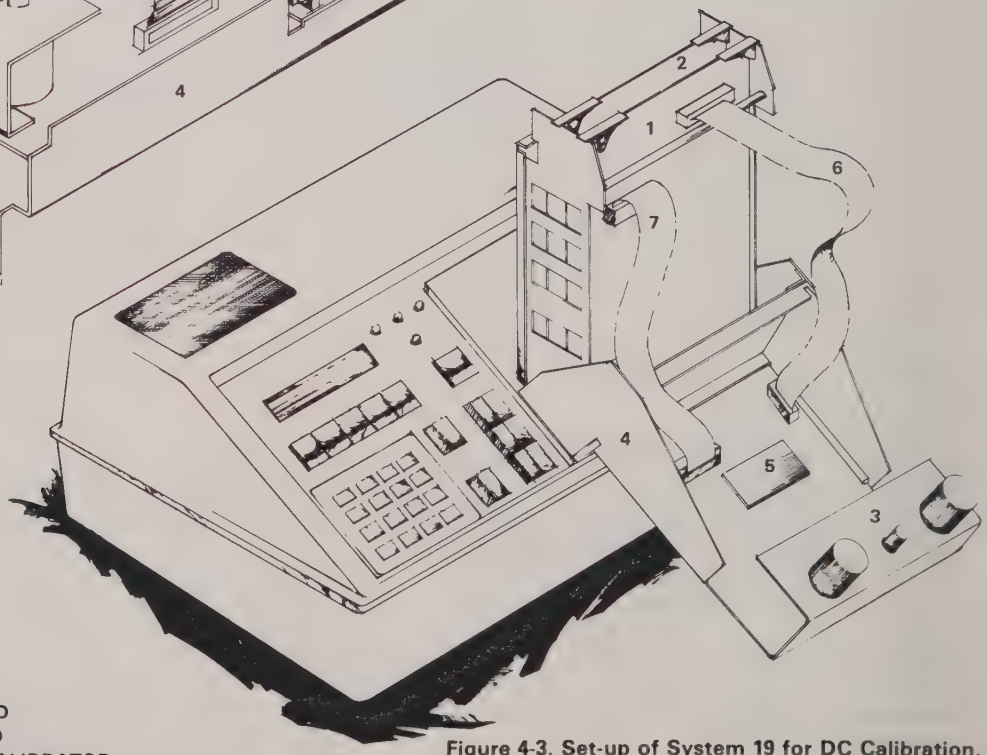


Figure 4-2. Set-up of Model 9 for DC Calibration.





1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration.

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE
To exit calibration, press:
SELECT
CØ (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

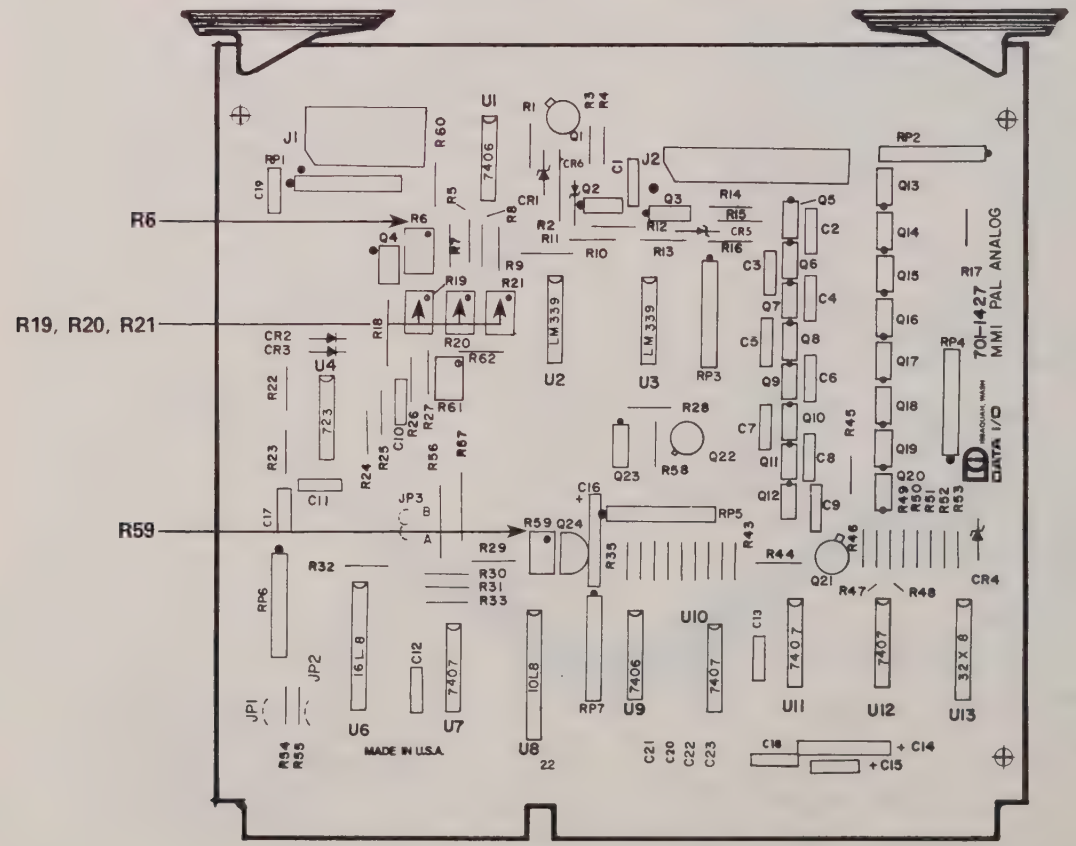


Figure 4-4. Analog Card Adjustment Locations

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

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CALIBRATION CHART 017-1427 — PROGRAM CARD 909-1427

FIXTURE 702-1071 — MANUFACTURER MMI

PAGE 1 OF 3 — PROGRAM ADAPTER 910-1427 — PROM PAL SERIES 20

DATE	REV	REVISION RECORD	DR	CK
5-15-78	A	RELEASE	GJ	
10-11-78	B	ECN # 2532	GB	
11-1-78	-	ECN # 2565	FS	
11-78	E	ECN #2568	GB	
7-14-80	E	ECN #3731	KJB	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
00	00	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	
00	00	+48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	Adjustments located on power supply board.
00	00	+5	1-3	000	00	000			+5	R18	5.05	5.10	5.15	See programmer manual.
00	00	-9	1-4	000	00	000			-9	R40	-8.8	-9.0	-9.2	
00	00	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		15.0		17.0	
20	02	VCC PROGRAM (1)	2-1	001	01	001	5	1	TP3	R21	10.5	11.0	11.5	*Adjustment Step.*
20	02	VCC CURRENT LIMIT	2-2	001	01	001	6	1	TP3		5.0		7.0	
20	04	VCC READ	2-3	002	02	002	5	1	TP3	R20	4.75	5.00	5.25	*Adjustment Step.*
00	00	VCC VERIFY VL	2-4	003	03	003	5	1	TP3	R19	4.3	4.5	4.7	*Adjustment Step.*
20	08	VCC VERIFY VH	2-5	004	04	004	5	1	TP3	R6	5.8	6.0	6.2	*Adjustment Step.*
20	08	COMPARATOR REF VH	3-1	004	04	004			U2 P8		1.6		2.0	Test point located on analog card.
00	00	COMPARATOR REF VL	3-2	005	05	005			U2 P8		0.8		1.2	
00	00	BIT 8 PROGRAM VHH SET (2)	4-1	005	05	005	4	8	TP3	R59	10.5	11.0	11.5	*Adjustment Step.*
00	00	VHH CURRENT LIMIT	4-2	005	05	005	6	8	TP3		2.5		4.6	
00	20	BIT 8 NO PROGRAM	4-3	006	06	006	2	8	TP3		2.35		2.70	
00	20	BIT 7 PROGRAM	4-4	006	06	006	4	9	TP3		10.5		11.5	
00	40	BIT 7 NO PROGRAM	4-5	007	07	007	2	9	TP3		2.35		2.70	
00	40	BIT 6 PROGRAM	4-6	007	07	007	4	10	TP3		10.5		11.5	
00	60	BIT 6 NO PROGRAM	4-7	008	08	010	2	10	TP3		2.35		2.70	
00	60	BIT 5 PROGRAM	4-8	008	08	010	4	11	TP3		10.5		11.5	
00	00	BIT 5 NO PROGRAM (8)	4-9	009	09	011	2	11	TP3		2.35		2.70	
80	01	BIT 8 COMPARATOR	5-1	010	0A	012	3	8						Confirm Bits 2, 3 and 4 ON (HEX E) on DO Bus.
80	01	BIT 7 COMPARATOR	5-2	010	0A	012	3	9						Confirm Bits 1, 3 and 4 ON (HEX D) on DO Bus.
80	01	BIT 6 COMPARATOR	5-3	010	0A	012	3	10						Confirm Bits 1, 2 and 4 ON (HEX B) on DO Bus.
80	01	BIT 5 COMPARATOR	5-4	010	0A	012	3	11						Confirm Bits 1, 2 and 3 ON (HEX 7) on DO Bus.
00	00	DATA DISABLE	5-5	011	0B	013								Confirm all Bits OFF (HEX 0) on DO Bus.
00	00	CLK/OD LINE 2 VHH	6-1	011	0B	013	4	2	TP3		10.5		11.5	
00	00	CLK/OD LINE 1 VIL (4)	6-2	011	0B	013	7	3	TP3		0.0		0.4	
00	10	CLK/OD LINE 1 VIH	6-3	012	0C	014	7	3	TP3		4.8		5.4	

COMMENTS
- Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below.
- Switch S1 must be depressed for accurate readings.
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CALIBRATION CHART . 017-1427

PAGE 2 OF 3

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	
00	00	BIT 4 PROGRAM	7-1	261	105	405	4	12	TP3		10.5		11.5	
00	20	BIT 4 NO PROGRAM	7-2	262	106	406	2	12	TP3		2.35		2.7	
00	20	BIT 3 PROGRAM	7-3	262	106	406	4	23	TP3		10.5		11.5	
00	40	BIT 3 NO PROGRAM	7-4	263	107	407	2	23	TP3		2.35		2.7	
00	40	BIT 2 PROGRAM	7-5	263	107	407	4	22	TP3		10.5		11.5	
00	60	BIT 2 NO PROGRAM	7-6	264	108	410	2	22	TP3		2.35		2.7	
00	60	BIT 1 PROGRAM	7-7	264	108	410	4	21	TP3		10.5		11.5	
00	00	BIT 1 NO PROGRAM	7-8	265	109	411	2	21	TP3		2.35		2.7	
80	01	BIT 4 COMPARATOR	8-1	266	10A	412	3	12						Confirm Bits 2, 3 and 4 ON (HEX E) on DO Bus.
80	01	BIT 3 COMPARATOR	8-2	266	10A	412	3	23						Confirm Bits 1, 3 and 4 ON (HEX D) on DO Bus.
80	01	BIT 2 COMPARATOR	8-3	266	10A	412	3	22						Confirm Bits 1, 2 and 4 ON (HEX B) on DO Bus.
80	01	BIT 1 COMPARATOR	8-4	266	10A	412	3	21						Confirm Bits 1, 2 and 3 ON (HEX 7) on DO Bus.
00	00	DATA DISABLE	8-5	267	10B	413								Confirm all Bits OFF (HEX 0) on DO Bus.
00	00	CLK/OD LINE 1 VHH	9-1	267	10B	413	4	3	TP3		10.5		11.5	
00	00	CLK/OD LINE 2 VIL (5)	9-2	267	10B	413	7	2	TP3		0.0		0.4	
00	10	CLK/OK LINE 2 VIH	9-3	268	10C	414	7	2	TP3		4.8		5.4	
00	00	IO VIL LEVEL (6)	10-1	000	00	000	7	20	TP3		0.0		0.4	
20	02	IO VIH LEVEL	10-2	001	01	001	7	20	TP3		4.8		5.4	
20	08	IO VHH LEVEL	10-3	004	04	004	4	20	TP3		10.5		11.5	
20	08	I1 VIL LEVEL (7)	10-4	004	04	004	7	19	TP3		0.0		0.4	
00	00	I1 VIH LEVEL	10-5	005	05	005	7	19	TP3		4.8		5.4	
00	60	I1 VHH LEVEL	10-6	008	08	010	4	19	TP3		10.5		11.5	
00	60	I2 VIL LEVEL	10-7	008	08	010	7	18	TP3		0.0		0.4	
00	00	I2 VIH LEVEL	10-8	009	09	011	7	18	TP3		4.8		5.4	
00	10	I2 VHH LEVEL	10-9	012	0C	014	4	18	TP3		10.5		11.5	
00	10	I3 VIL LEVEL	10-10	012	0C	014	7	17	TP3		0.0		0.4	
00	00	I3 VIH LEVEL	10-11	013	0D	015	7	17	TP3		4.8		5.4	
00	00	I3 VHH LEVEL	10-12	016	10	020	4	17	TP3		10.5		11.5	
00	00	I4 VIL LEVEL	10-13	016	10	020	7	16	TP3		0.0		0.4	
00	00	I4 VIH LEVEL	10-14	017	11	021	7	16	TP3		4.8		5.4	
00	00	I4 VHH LEVEL	10-15	020	14	024	4	16	TP3		10.5		11.5	
00	00	I5 VIL LEVEL	10-16	020	14	024	7	15	TP3		0.0		0.4	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
00	00	I5 VIH LEVEL	10-17	021	015	025	7	15	TP3		4.8		5.4
00	00	I5 VHH LEVEL	10-18	024	018	030	4	15	TP3		10.5		11.5
00	00	I6 VIL LEVEL	10-19	024	018	030	7	14	TP3		0.0		0.4
00	00	I6 VIH LEVEL	10-20	025	019	031	7	14	TP3		4.8		5.4
00	00	I6 VHH LEVEL	10-21	028	01C	034	4	14	TP3		10.5		11.5
00	00	I7 VIL LEVEL	10-22	028	01C	034	7	13	TP3		0.0		0.4
00	00	I7 VIH LEVEL	10-23	029	01D	035	7	13	TP3		4.8		5.4
00	00	I7 VHH LEVEL	10-24	032	020	040	4	13	TP3		10.5		11.5
00	00	CONFIGURE LINE 1	11-1	032	020	040	7	6	TP3		4.8		5.4
00	00	CONFIGURE LINE 2	11-2	032	020	040	7	7	TP3		4.8		5.4
00	00	GND	11-3	032	020	040	8	24	TP3		0.0		0.08
00	00	DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1427

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop.
	b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START.
	b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:
	a. Ground J1-16 on the analog card.
	b. Press LOAD.
	c. Press EXECUTE.
	d. Press KEYBOARD.
	e. Key in data — Ø hex — at address ØØ1.
	f. Press VERIFY.
	g. Press EXECUTE. The programmer will mis-verify

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) When using a Model 9, always key in the hex data in parentheses to be sure that the correct data is placed on the DI bus.

Revision "A" Software: Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in hex data called out in parentheses on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software: With the KEYBOARD indicator illuminated and all the others OFF, use the hex keypad to key in hex data called out in parentheses on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the hex data in parentheses into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5: Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF. Ignore the hex data on the chart.

Model 9: With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19: With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Check the Timing Diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

d. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

e. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

f. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

g. Reinstall the digital card in the slot from which it was removed.

h. Check the NOTES column on the Timing Diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1—5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the Timing Diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1—5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display. Return to address ØØØ.
Model 9:	Enter hex data "Ø1" at several addresses. Return to address ØØØ.
System 19:	Enter hex data "Ø1" at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the Timing Diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets. Return to address ØØØ.

4. Select the PROGRAM mode:

Models 1—5, press:	RESET PROGRAM AUTO RAM-ROM2

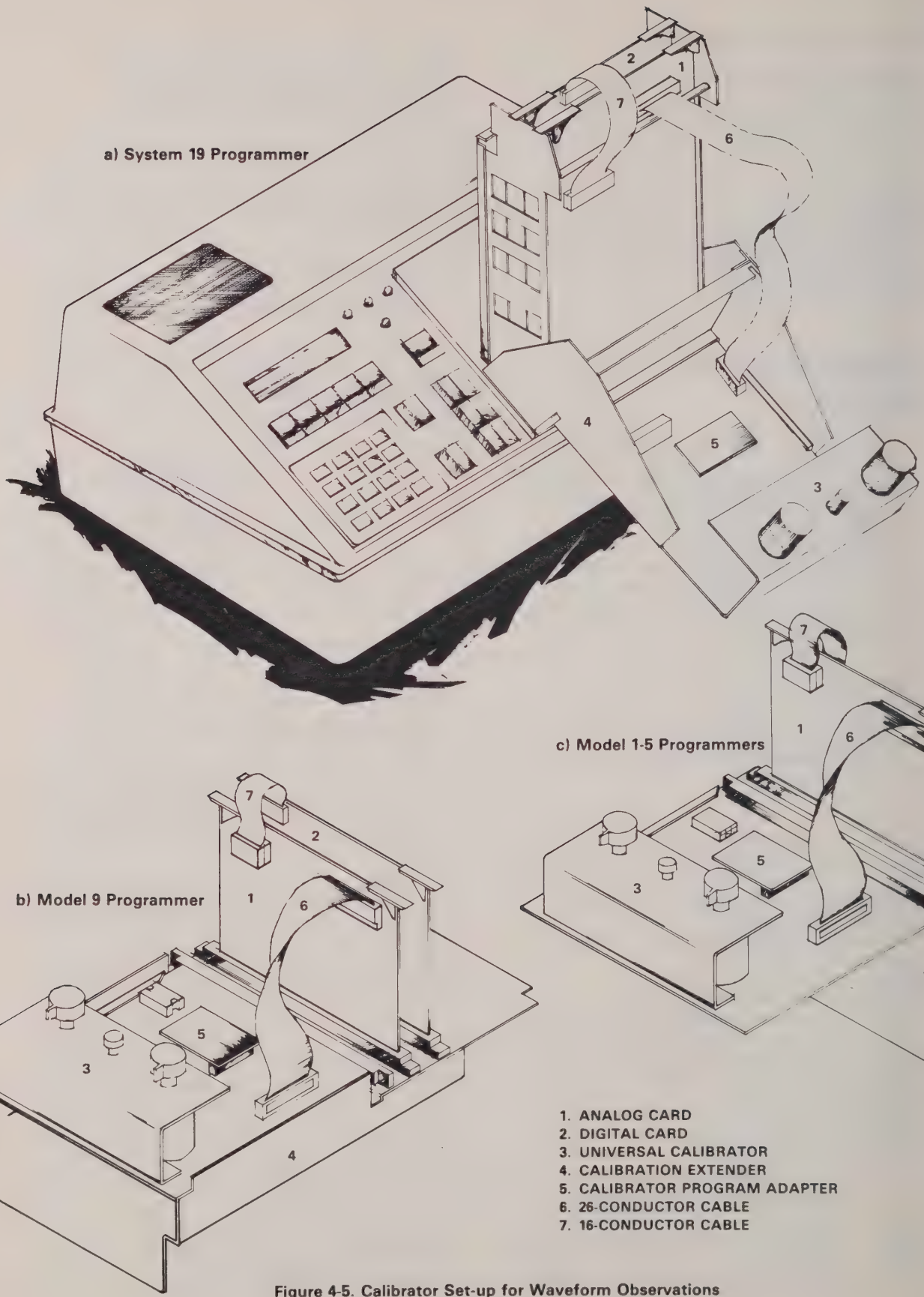
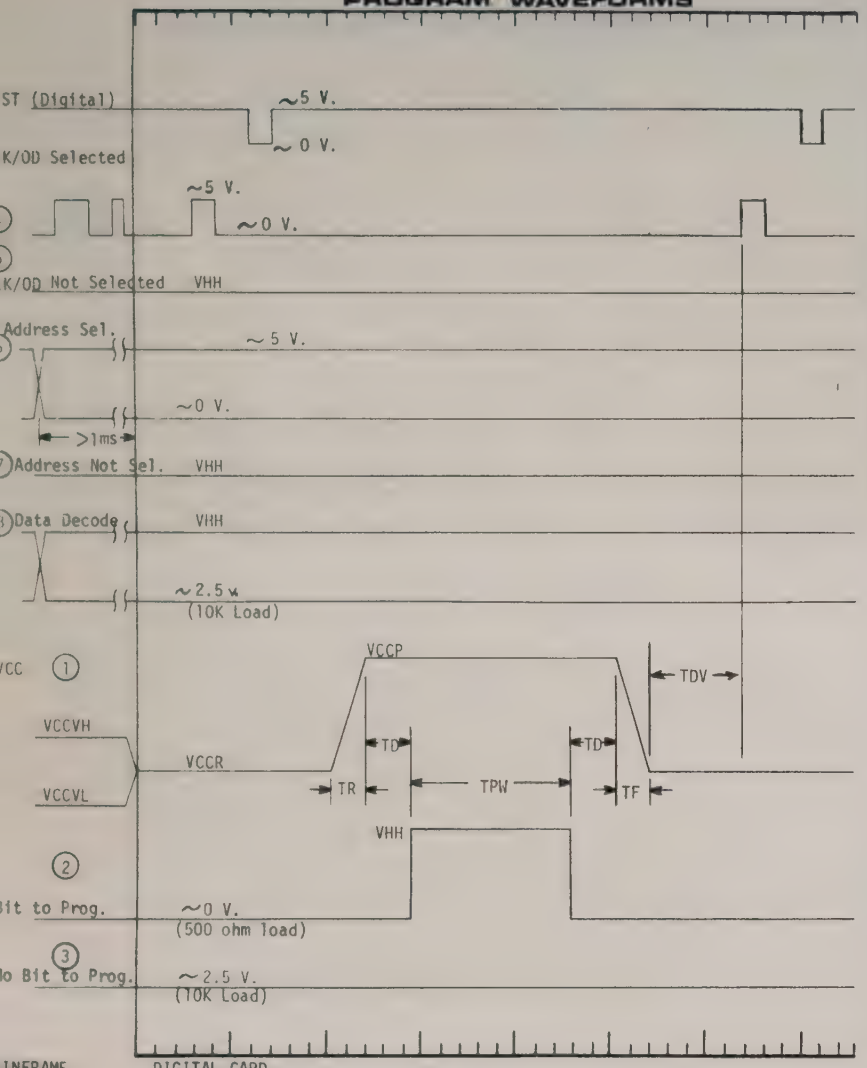


Figure 4-5. Calibrator Set-up for Waveform Observations

PROGRAM WAVEFORMS



NOTES

1454

DIGITAL CARD JUMPERS

JP1 = SHORT
JP2 = SHORT
JP3 = SHORT
JP4 = SHORT
JP5 = SHORT
JP6 = SHORT
JP7 =OPEN
JP8 = C = 5 Pulse Reject
JP8 = M = 1 Pulse Reject
JP9 = B
JP10 = OPEN
JP11 = 512 = WORD LIMIT

Clk Rate (CR3) = (omit)
Clk Rate (CR4) = (omit)

WAVEFORM VARIABLES

VHH = 11.0 volts ± 0.5 V.
VCCR = 5.00 ± 0.25 V.
TD > 100 ns
TR = TF = 1 to 20 us
TPW = 45 ± 5 us
TPW Duty Cycle 25% max.
VCC VL = 4.5 ± 0.2 V.
VCC VH = 6.00 ± 0.2 V.
VCCP = 11.0 ± 0.5 V.
TDV > 100 us

(1) These waveforms correspond to callouts on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

For calibration, the card set polarity defaults to VOH.

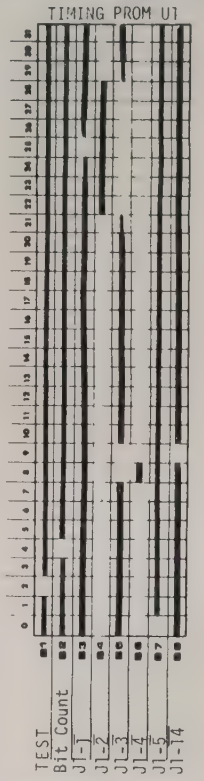
DATE	SYM	REVISION RECORD	DR.	CK.
2-79 Rev. 6-79 F		ECN#2594 5-25-78 ECN#2997	VS	
5-78	A	RELEASE	VS	
8-78	B	CN 2383	GB	
10-78	C	CN 2532	GB	
11-78	E	CN 2568	GB	

FS

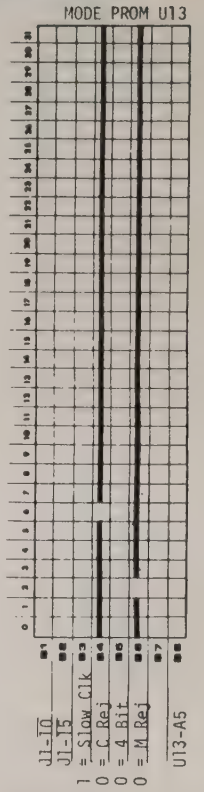
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

TIMING PROM U1



MODE PROM U13



DATA I/O ISSAQUAH, WASH.

Timing Diagram

DRAWN BY G. James

APPROVED BY

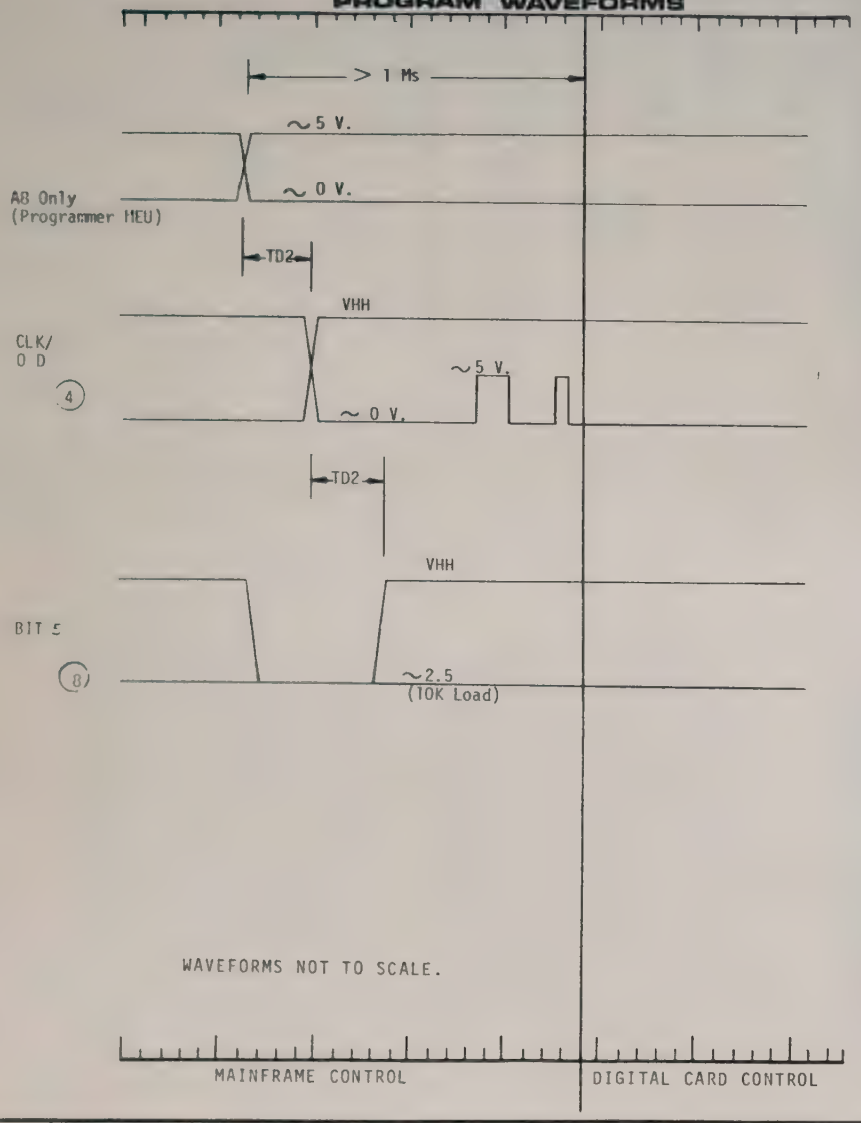
TITLE M.M.I. PAL

DATE 5-25-78

DRAWING NUMBER 007-1427 1 OF 2

DATE	BY	REVISION RECORD	BR.	CH
6/79	F	ECN# 2997		

PROGRAM WAVEFORMS



NOTES

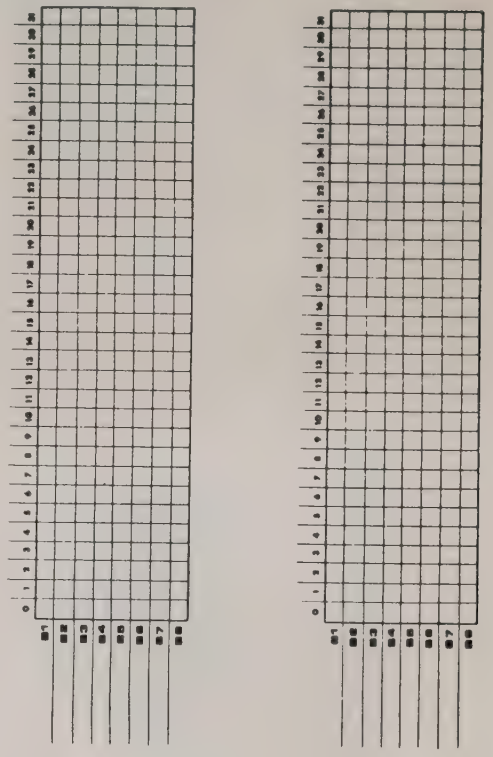
For calibration, the card set polarity defaults to VOH.

TD2 = 5 to 50 us

(Refer to the Clock/OD Drivers section on page 4-5 of the Instruction Manual for an explanation of the waveforms)

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)



DATA I/O ISSAQUAH, WASH.

TIMING DIAGRAM	DRAWN BY G. James
	APPROVED BY
TITLE M.M.I. PAL	
DATE 8-8-78	DRAWING NUMBER 007-1427 Sheet 2 of 2

Model 9, press:	PROGRAM
System 19, press:	SELECT C1 START PROG

5. Initiate waveforms:

Models 1—5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1—5 and 9, press:	STOP
System 19, press	KEYBD

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

CAUTION

The reject jumper must be reinstalled. Otherwise, the device's programming specifications will be violated, and the programmer and/or cardset may be damaged by a prolonged attempt to program a defective device.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Repeat the key sequence in Waveform Test Procedure, paragraph 4.4.2, steps 1—5.
6. With Universal Calibrator switch positions selected to observe the test pulse waveform, repeat step 6 of the Test Procedure. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative.

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram, contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the device being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the device being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the device on the DO Bus. These data are compared at each bit of each device word both before and after programming. At each bit, the digital card continues to command device program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of device manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed device bit is tested for loading and/or leakage. Following the program cycle, devices are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

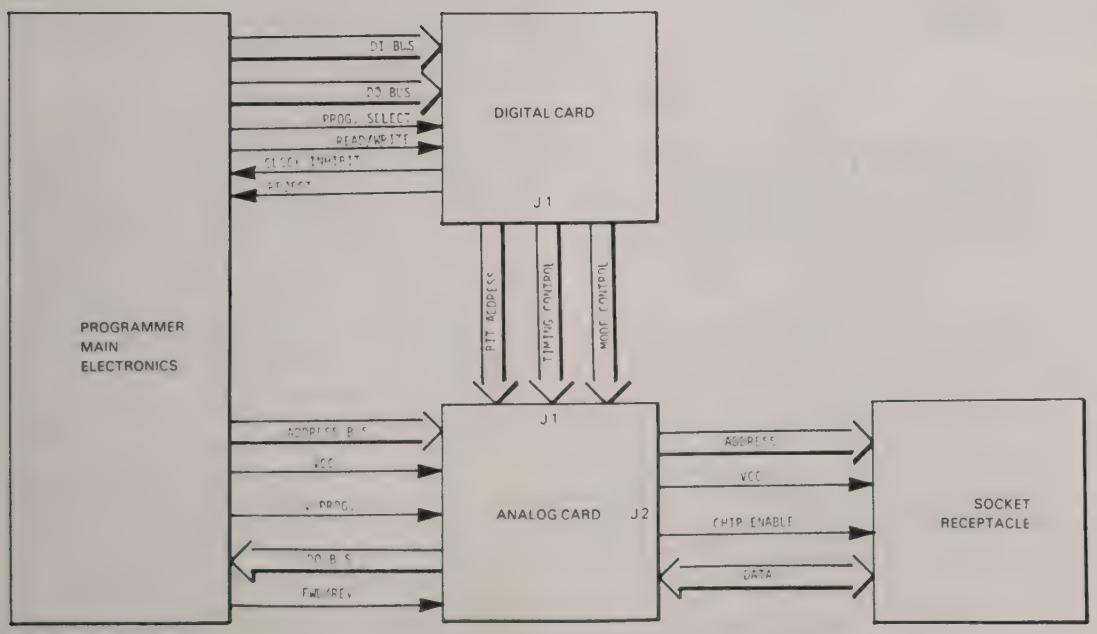


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

Figure 5-2 gives a generalized block diagram of the digital card. This diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnection information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.1 SELECT GATES

U15 and U16 (on schematic) monitor Program Select (LL), Write Inhibit (PP), Read (X), and Read Inhibit (RR) in order to enable operation of the digital card. Output from Read Gate U15 is routed to the analog card to control the Data Bus Drivers. The Write Output Enable Gate allows the Program Memory to be set.

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a Write command on AA. This causes the Sequence Counter on the digital card to begin operation and halts the programmer. Initialization of the Program Pulse Counter, Bit Counter and Sequence Counter and clearing of the Overprogram Counter occur before the Program Memory is set.

5.2.3 CLOCK GENERATOR

The clock is always running. When the Program Memory sets in response to the Write and Program Select commands, the programmer is inhibited and the Sequence Counter Load line is released, allowing the counter to recognize clock pulses. Alternate clock rates are determined by the Mode ROM or by the High Order (H/O) Memory (with JP7 connected).

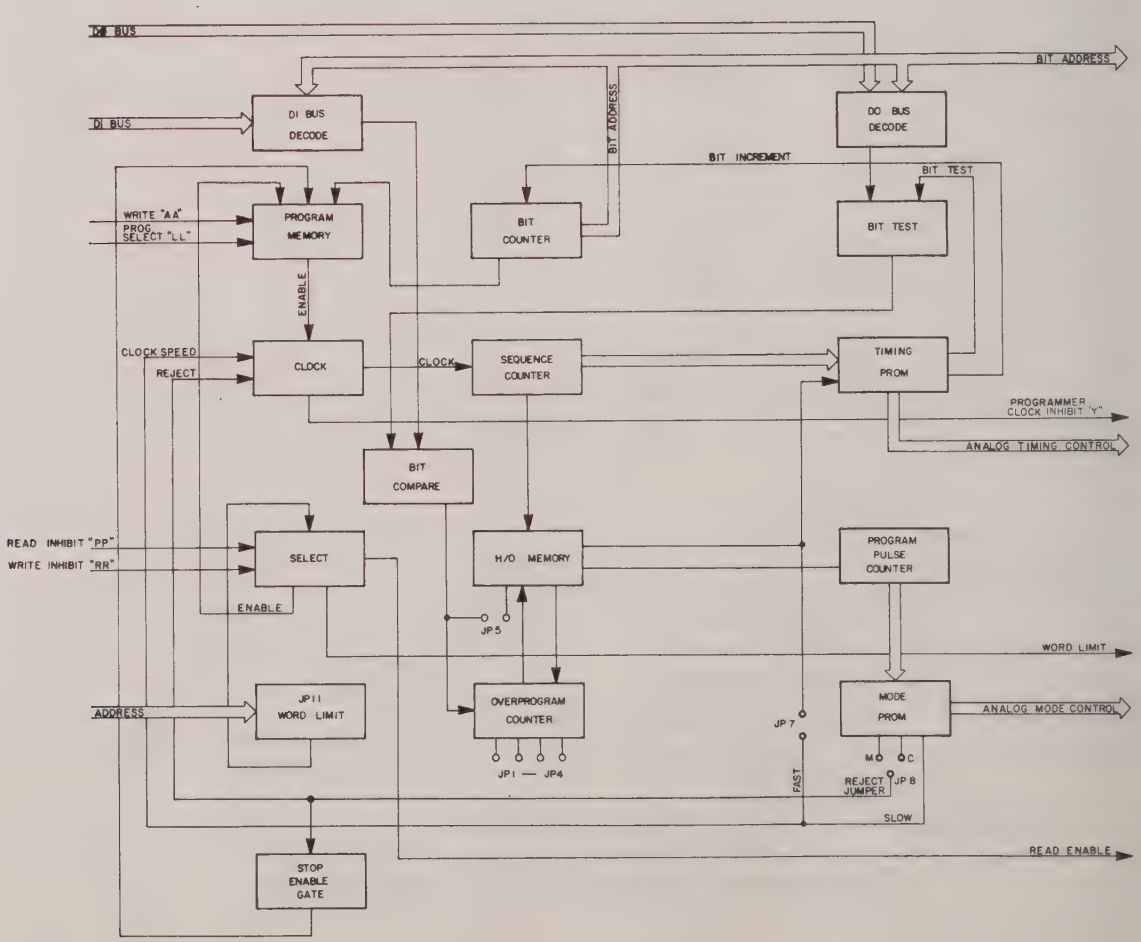


Figure 5-2. Block Diagram, 1454 Digital Card.

5.2.4 SEQUENCE COUNTER

The 4-bit Sequence Counter drives the 32x8 Timing ROM. The combination generates Bit Test and Bit Increment pulses, which are used on the digital card, as well as timing signals for analog control, which are clocked through a latch to the interface connector. (See the Timing Diagram.)

5.2.5 TIMING ROM

Output words from the Timing ROM are used in the serial Verify and Program operations, as shown in the Timing Diagram. Verify operations use Low Order words 0 to 15; Program operations use High Order words 16 through 31. Words 8 through 11 are used to output control signals for Vcc voltages during Read and Verify operations, which occur under machine control when the digital card is not selected. Those words are loaded through the Sequence Counter to the Timing ROM, as determined by the FWD line and Write Inhibit. (See the Schematic.)

At the beginning of a programming sequence (word 2), the Timing ROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PAL, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

5.2.6 OVERPROGRAM COUNTER

The Bit to Program pulse loads the Overprogram Counter and also sets the Bit to Program Memory. This, in turn, allows a carry pulse from the Sequence Counter to reach the high order memory. It also disables the Bit Count Gate until the Overprogram Counter clocks the Zit to Program Memory after the bit has been programmed.

At Timing ROM word 15, the carry pulse from the Sequence Counter toggles the H/O memory. This enables the fifth address line to the Timing ROM, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to again toggle the H/O memory. This sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing ROM; if the buses compare at Bit Test (bit is programmed), the output of the Bit Compare Gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count Gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes a High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP1—JP4. The borrow pulse resets the Bit to Program Memory which enables the Bit Count Gate, allowing it to decrement the bit count to the next bit.

Some cards are wired with JP5 shorted. With JP5 shorted, a Bit to Program pulse sets the High Order Memory. This causes the fifth address input line to the Timing ROM to go high, enabling the programming sequence of the Timing ROM. At word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP5 shorted, the total sequence is 16 pulses long.

5.2.7 PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PAL being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode ROM. The Timing Diagram includes the truth table for the Mode Control ROM. Outputs of the Mode ROM control the magnitude of the program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 6 control the number of programming attempts allowed before a reject is signalled to the programmer; reject jumper JP8 selects either the M line or the C line. (See the Timing Diagram for the pulse numbers selected.)

5.2.8 BIT COUNTER

The Bit Counter counts bit increment pulses arriving from the Timing ROM through the Bit Counter Gate. This gate is disabled, halting the Bit Counter when the Bit to Program Memory is set by a Bit-to-Program pulse. The Bit Counter counts down from either 4 or 8, as determined by the socket adapter or the Mode ROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder as well as the Bit Decoder on the Analog Card. When the Bit Counter reaches zero, its borrow output is used to reset the Program Memory.

5.2.9 WORD LIMIT SELECT

Word Limit is jumper-selected at JP11 on the digital card to 256, 512, 1024, or 2048. JP10 limits the address range of the programmer through the Word Limit line (CC), according to the configuration of the device being programmed. Selection defaults to the socket adapter.

5.3 ANALOG CARD

Figure 4-3 gives a generalized block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnection information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions contained on the analog card.

5.3.1 ADDRESS DECODE

The Address Decode accommodates address lines A_2, A_3 and A_4 from the programmer MEU, performing a 1-of-8 decode. The decoder is a 32x8 tri-state ROM that sends its outputs to the Address Buffers.

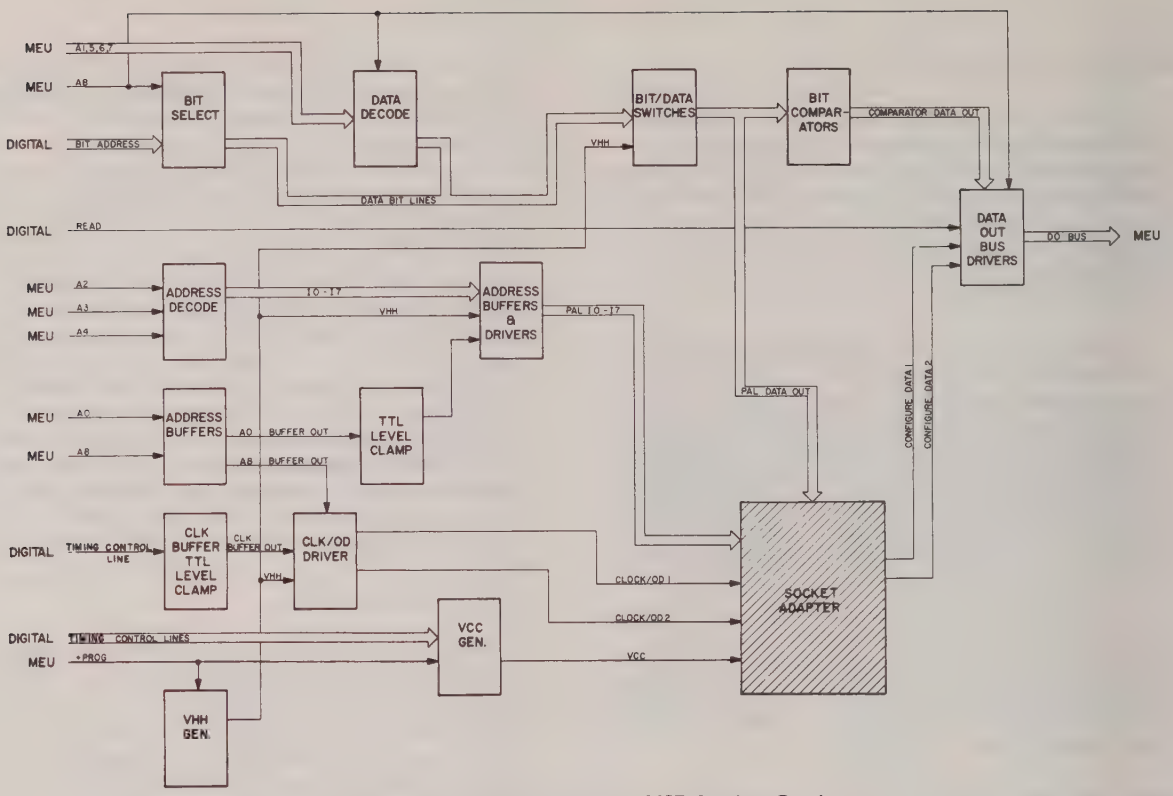


Figure 5-3. Block Diagram, 1427 Analog Card.

5.3.2 ADDRESS BUFFERS AND DRIVERS

The Address Buffers are 8 noninverting gates with high-voltage uncommitted collector outputs. These outputs control the Address Drivers.

The Address Drivers are three-level drivers which provide the specified levels to inputs I_0 through I_7 of the PAL being programmed. Each driver is a PNP switch tied to the V_{HH} supply. The switches, when turned on, set inputs I_0 through I_7 to the V_{HH} level. When off, the I_0 through I_7 levels are held to TTL levels by the TTL Level Clamp.

5.3.3 TTL LEVEL CLAMP

This circuit serves as a 2-level clamp to the Address Drivers. The 2 levels are TTL "1" and TTL "0" voltages. These levels are selected by address line A_8 (programmer MEU) and generated by a transistor saturation voltage and zener diode clamp. This clamp is tied to the Address Drivers by load resistors.

5.3.4 CLOCK BUFFER

The Clock Buffer is an inverting gate with an uncommitted collector output. Its input is from the digital card via pin 5 of the J1 interface connector. The output controls the TTL clamp. This TTL clamp circuit is identical to the address TTL clamp. It clamps the CLK/OD lines to TTL levels via load resistors.

5.3.5 CLOCK/OD DRIVERS

The three-level Clock/OD Drivers are PNP switches which control the specified levels to the Clock/OD inputs of the PAL. The switches, when ON, set the clock/OD lines to the V_{HH} level. When the switches are OFF, the Clock/OD lines are clamped to TTL levels by the TTL Level clamp.

Buffered address line A_8 is delayed to $A_{8'}$ which controls the Clock/OD Driver PNP switches. This delay allows address line A_8 to stabilize before the Clock/OD lines switch. $A_{8'}$ is further delayed to $A_{8''}$ which controls the Data Decode and Bit Select PAL (U8). This second delay ensures that the Clock/OD lines have stabilized before allowing the Data Decode and Bit Select PAL to enable the Bit/Data Switches.

5.3.6 V_{HH} GENERATOR

The V_{HH} Generator is a current-limited voltage regulator that supplies the specified V_{HH} voltage to the address, CLK/OD and data lines. The generator consists of an adjustable shunt regulator with an emitter follower pass transistor. The regulator output is adjustable using potentiometer R59.

5.3.7 V_{CC} GENERATOR

The V_{CC} Generator is a current-limited voltage regulator with four selectable states. The V_{CC} Program status is

selected while programming pulses are being applied to the device. The V_{CC} Verify states are selected while the programmer is performing FWD and REV Verify operations. The V_{CC} Read state is selected while the programmer is performing load operations.

An IC voltage regulator and pass transistor make up the V_{CC} generator. The regulator input voltage is supplied by the programmer + PROG Supply.

5.3.8 DATA DECODE AND BIT SELECT

Data Decode and Bit Select functions are accomplished by a PAL (U8). This circuit controls the Bit/Data switches. They take inputs from the programmer MEU address lines A_1, A_5, A_6, A_7 and A_8, and from the Bit Address lines of the digital card.

5.3.9 BIT/DATA SWITCHES

These switches provide the PAL output bit lines with the specified levels during Verify and Program operations.

The Data Decode circuitry controls the bit switches for PAL bit lines that are to be decode inputs. The Bit Select circuitry controls the bit switches for PAL bit lines that are to receive program pulses. The program pulse width is controlled via the chip select input of the bit select PAL. This timing signal is generated on the digital card and is routed to the analog card via the interface connector J1.

5.3.10 BIT COMPARATOR AND DATA OUT BUS DRIVER

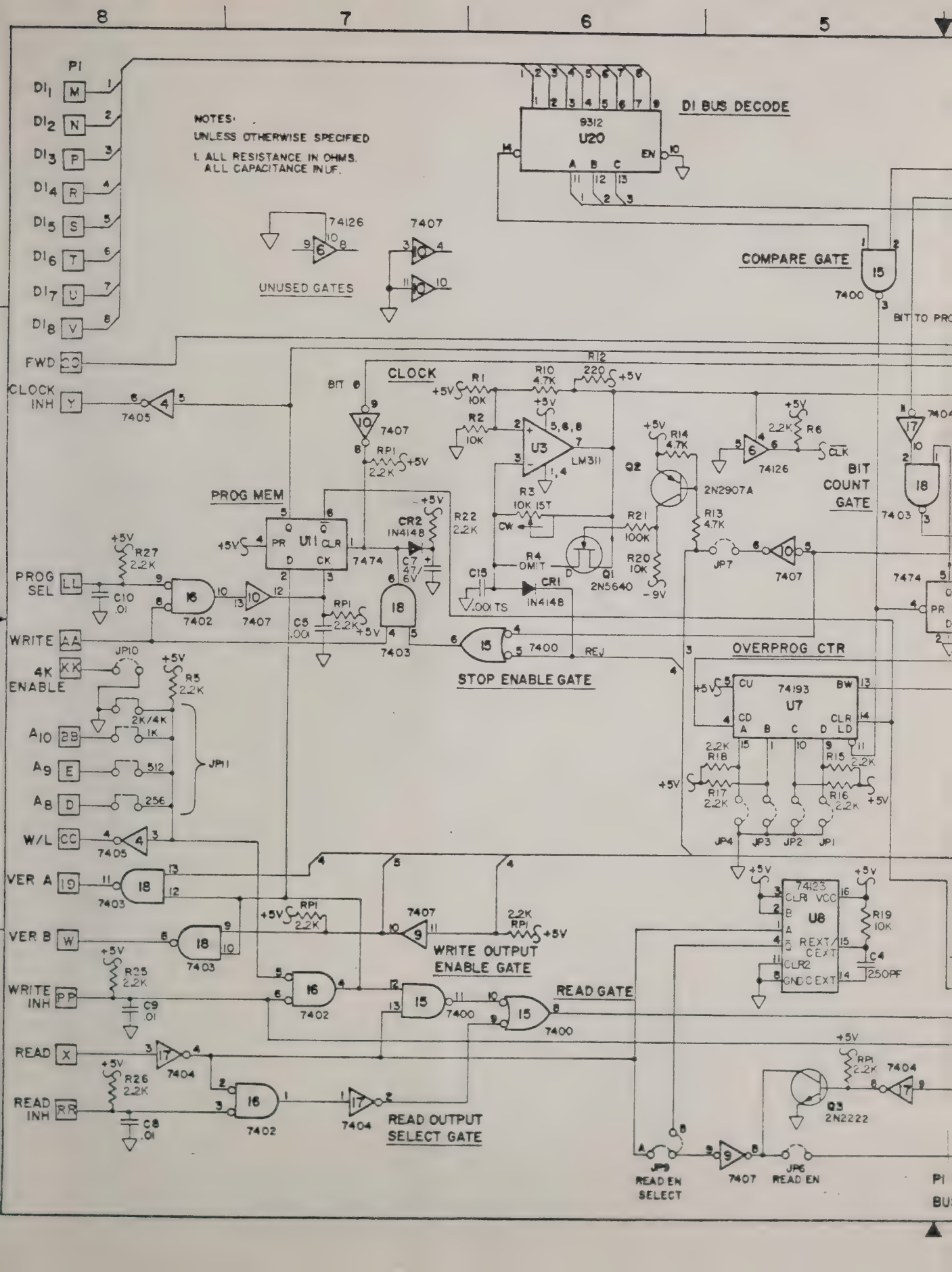
The Bit Comparator compares the PAL's programmed data against a reference level. During Read, comparator outputs are transferred to the Data Out Bus Driver (U6). This transfer allows the digital card to compare the PAL output (DO Bus) and the programmer DI Bus. The DO Bus Drivers are selected as inverters or noninverters by the socket adapter configure lines. For VOH adapters, the driver is configured to invert and for VOL it is configured not to invert.

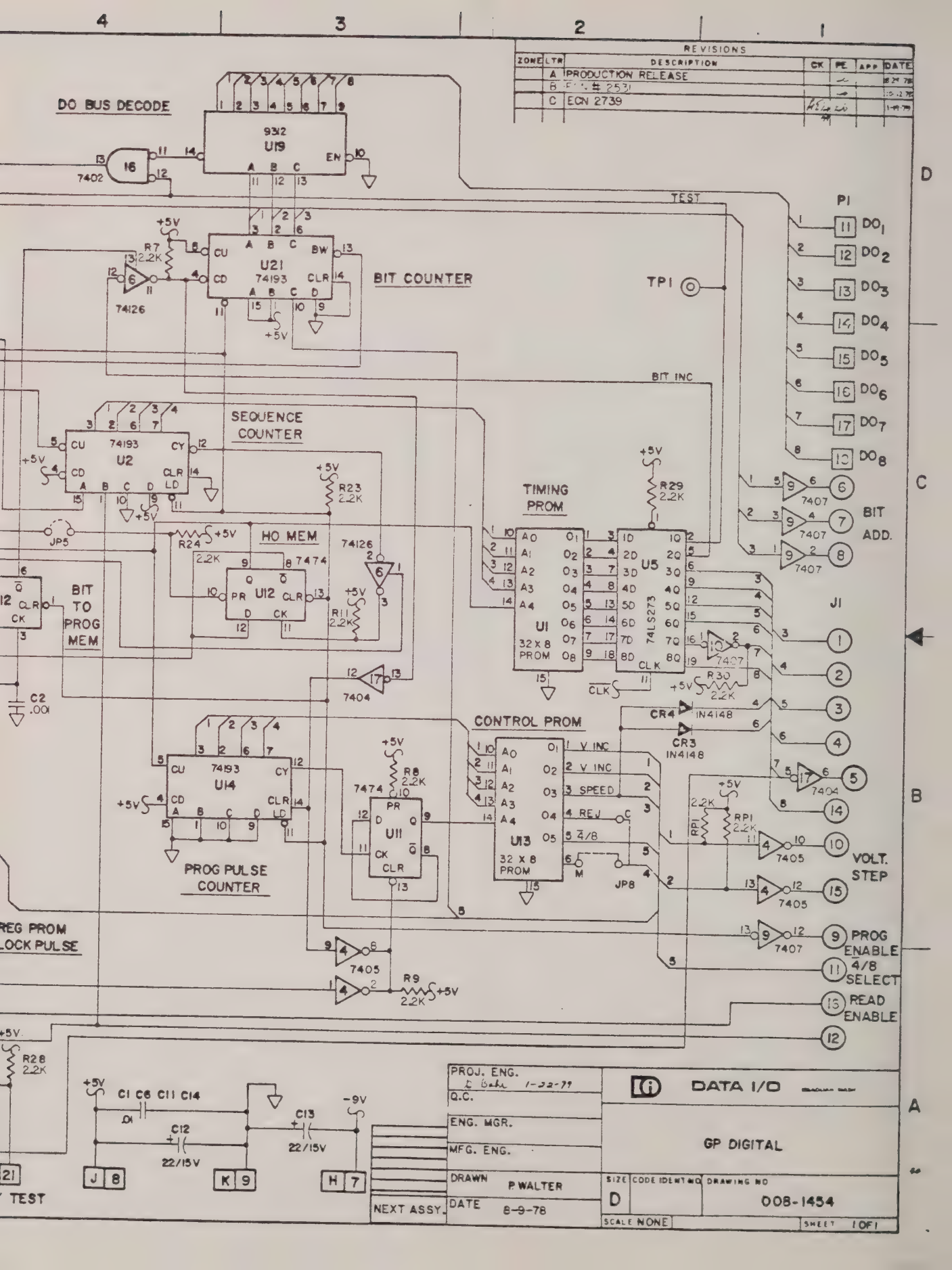
The driver multiplexes the eight PAL bit lines down to 4 DO Bus lines when VOL or VOH socket adapters are used. When a VOL/VOH adapter is used, the driver outputs only 2 DO Bus lines.

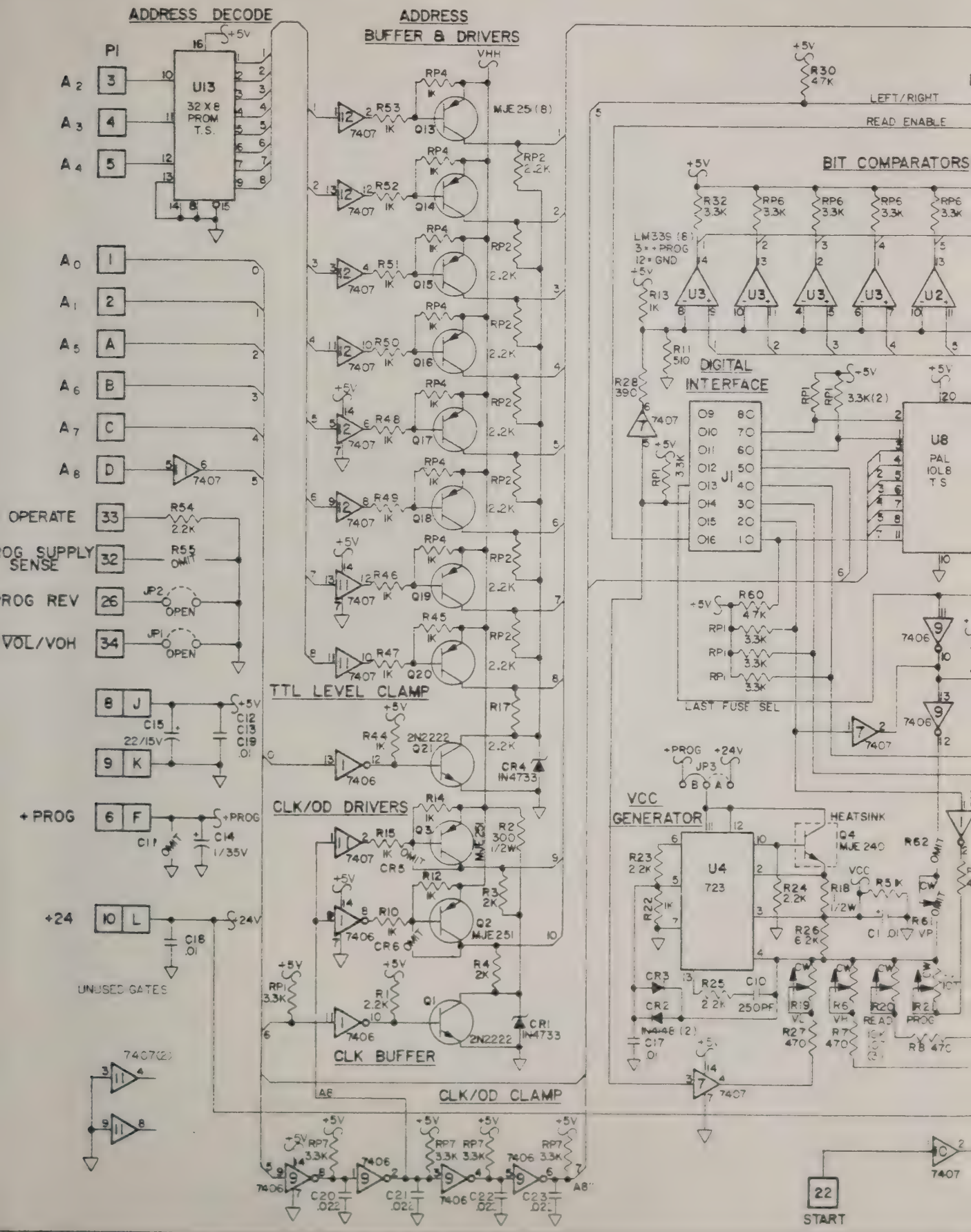
This driver is controlled by MEU address line A_8, the digital card read line, and the socket adapter configure lines.

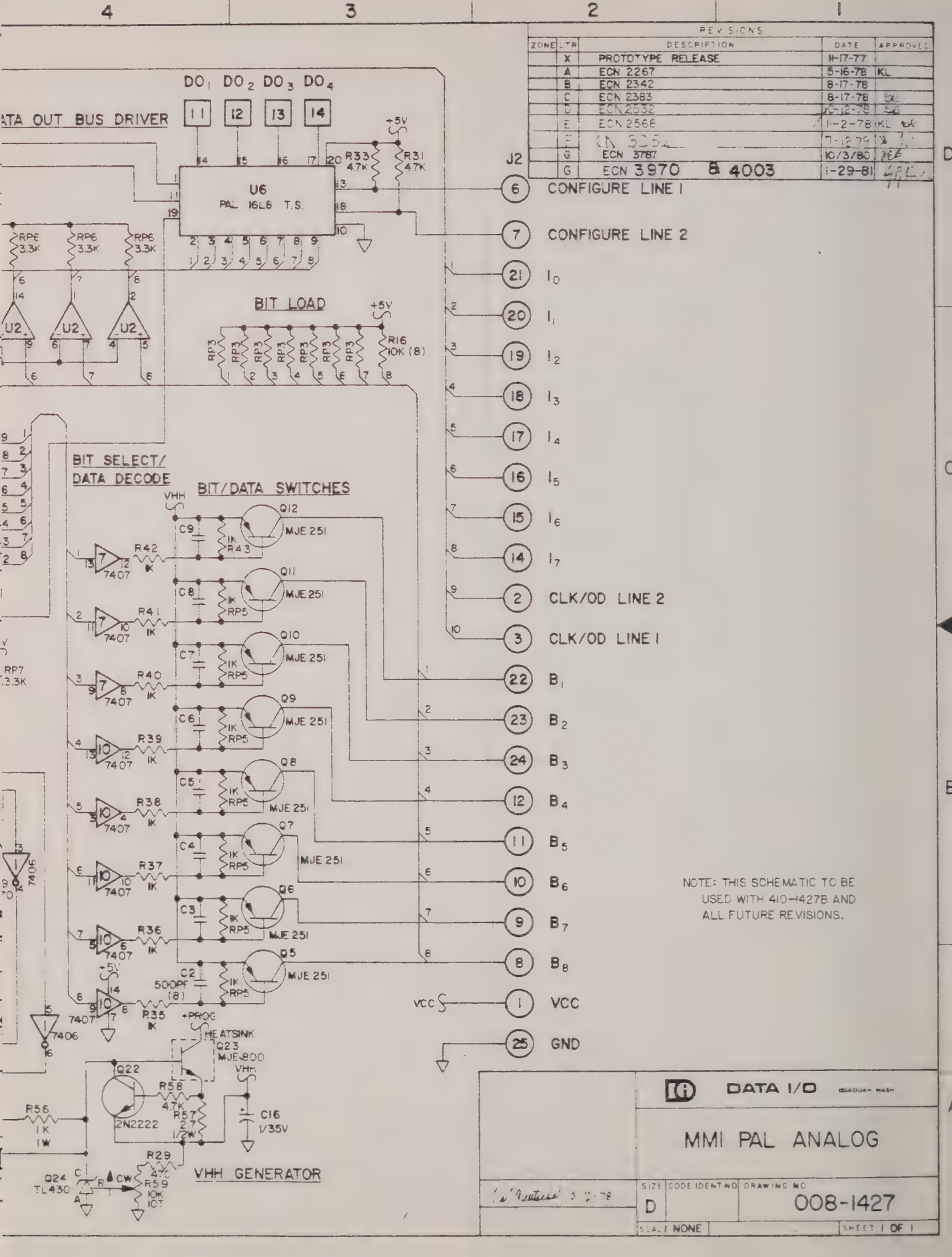
SECTION 6
SCHEMATICS

008-1454	GP Digital
008-1427	MMI PAL Analog
010-1427	Truth Table
008-1072	Plug In Adapter

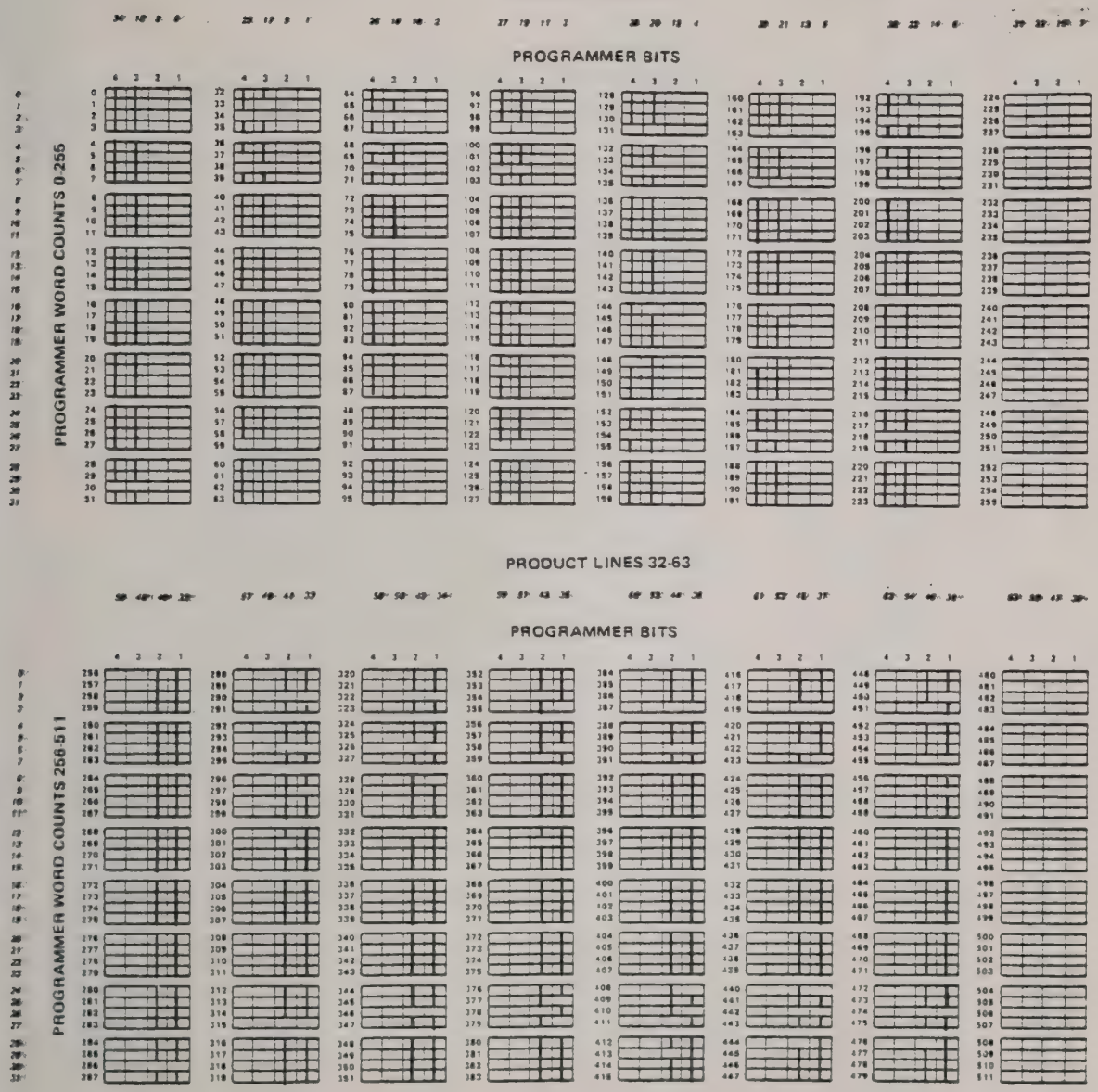

8
7
6
5
P1
DI1 M 1
DI2 N 2
DI3 P 3
DI4 R 4
DI5 S 5
DI6 T 6
DI7 U 7
DI8 V 8
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS.
ALL CAPACITANCE IN UF.
DI BUS DECODE
9312
U20
EN
A B C
UNUSED GATES
74126
7407
COMPARE GATE
7400
BIT TO PRO
FWD CC
CLOCK INH Y
7405
CLOCK
BIT 0
R1 10K
R2 10K
R10 4.7K
R12 220
+5V
RPI 2.2K
U3
LM311
5,8,6
1,4
R3 10K 15T
CW
R4 OMIT
C15 .001 TS
CR1 IN4148
Q1 2N5640
R21 100K
R20 10K
-9V
R14 4.7K
Q2 2N2907A
R13 4.7K
JP7
R6 2.2K
CLK
BIT COUNT GATE
7403
7474
PROG MEM
U11
PR CLR D CK
CR2 IN4148
R22 2.2K
C7 47/6V
PROG SEL LL
R27 2.2K
C10 .01
7402
7407
C5 .001
WRITE AA
4K ENABLE KK
JP10
R5 2.2K
2K/4K
1K
A10 BB
A9 E
A8 D
512
256
JP11
STOP ENABLE GATE
REJ
OVERPROG CTR
74193
U7
CU CD CLR
A B C D LD
BW
R18 2.2K
R17 2.2K
R15 2.2K
R16 2.2K
JP4 JP3 JP2 JP1
W/L CC
VER A 19
VER B W
WRITE INH PP
R25 2.2K
C9 .01
WRITE OUTPUT ENABLE GATE
READ GATE
74123
U8
CLR VCC
REXT/CEXT
CLR2
GND CEXT
R19 10K
C4 250PF
READ X
READ INH RR
R26 2.2K
C8 .01
7404
READ OUTPUT SELECT GATE
Q3 2N2222
JP9 READ EN SELECT
JP6 READ EN
P1 BU


REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
A PRODUCTION RELEASE
B ECN # 2531
C ECN 2739
DO BUS DECODE
9312
U19
7402
TEST
P1
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
+5V
R7 2.2K
U21
74193
BIT COUNTER
74126
TP1
BIT INC
SEQUENCE COUNTER
U2
R23 2.2K
TIMING PROM
R29 2.2K
U5
74LS273
U1
32X8 PROM
7407
BIT ADD.
JP5
R24 2.2K
HO MEM
7474
U12
74126
BIT TO PROG MEM
R11 2.2K
J1
C2 .001
7404
CR4 IN4148
CR3 IN4148
CONTROL PROM
U13
32 X 8 PROM
V INC
V INC
SPEED
REV
4/8
M
JP8
U14
74193
PROG PULSE COUNTER
R8 2.2K
U11
7474
RP1 2.2K
7405
VOLT. STEP
REG PROM
LOCK PULSE
R9 2.2K
PROG ENABLE
4/8 SELECT
READ ENABLE
R28 2.2K
C1 C6 C11 C14
.01
C12
22/15V
C13
22/15V
-9V
J 8
K 9
H 7
TEST
PROJ. ENG. E Bahr 1-22-79
Q.C.
ENG. MGR.
MFG. ENG.
DRAWN P WALTER
DATE 8-9-78
NEXT ASSY.
DATA I/O
GP DIGITAL
SIZE D
CODE IDENT NO
DRAWING NO 008-1454
SCALE NONE
SHEET 1 OF 1


ADDRESS DECODE
ADDRESS BUFFER & DRIVERS
P1
U13 32 X 8 PROM T.S.
A2
A3
A4
A0
A1
A5
A6
A7
A8
OPERATE
PROG SUPPLY SENSE
PROG REV
VOL/VOH
+PROG
+24
UNUSED GATES
7407(2)
VHH
RP4 1K
RP2 2.2K
R53 1K
R52 1K
R51 1K
R50 1K
R48 1K
R49 1K
R46 1K
R45 1K
R47 1K
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
MJE25(8)
TTL LEVEL CLAMP
R44 1K
2N2222 Q21
R17 2.2K
CR4 IN4733
CLK/OD DRIVERS
R14 1K
R15 1K
CR5
R12 1K
R10 1K
CR6
Q3
Q2 MJE251
R2 300 1/2W
R3 2K
R4 2K
R1 2.2K
Q1 2N2222
CR1 IN4733
CLK BUFFER
CLK/OD CLAMP
RP7 3.3K
C20 .022
C21 .022
C22 .022
C23 .022
A8"
R54 2.2K
R55 OMIT
JP2 OPEN
JP1 OPEN
C15 22/15V
C12 C13 C19 .01
C11 OMIT
C14 1/35V
C18 .01
LEFT/RIGHT
READ ENABLE
BIT COMPARATORS
R30 47K
R32 3.3K
LM339 (8)
3 = +PROG
12 = GND
R13 1K
R11 510
DIGITAL INTERFACE
R28 390
RPI 3.3K(2)
J1
U8 PAL 10L8 T S
R60 4.7K
LAST FUSE SEL
JP3
VCC GENERATOR
HEATSINK
Q4 MJE 240
U4 723
R23 2.2K
R22 1K
R24 2.2K
R18 1/2W
R5 1K
R62 OMIT
R26 6.2K
R6 VP
CR3
CR2
IN4148 (2)
R25 2.2K
C10 250PF
C17 .01
R19 VC
R27 470
R7 VH 470
R20 READ
R21 PROG
R8 470
22 START


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
X PROTOTYPE RELEASE 11-17-77
A ECN 2267 5-16-78 KL
B ECN 2342 8-17-78
C ECN 2383 8-17-78
D ECN 2532 10-12-78
E ECN 2568 11-2-78 KL
F ECN 3254 7-13-79
G ECN 3787 10/3/80
G ECN 3970 & 4003 1-29-81
DO1 DO2 DO3 DO4
ATA OUT BUS DRIVER
U6
PAL 16L8 T.S.
+5V
R33 4.7K
R31 4.7K
RP6 3.3K
U2
BIT LOAD
RP3
R16 10K (8)
BIT SELECT/
DATA DECODE
BIT/DATA SWITCHES
VHH
Q12
Q11
Q10
Q9
Q8
Q7
Q6
Q5
MJE 251
C9
C8
C7
C6
C5
C4
C3
C2 500PF (8)
1K RP5
1K R43
R42
R41
R40
R39
R38
R37
R36
R35 1K
7407
7406
+PROG
HEATSINK
Q23 MJE-800
Q22 2N2222
R58 4.7K
R57 2.7 1/2W
C16 1/35V
R56 1K 1W
R29 4K
R59 10K 10T
Q24 TL430
VHH GENERATOR
J2
6 CONFIGURE LINE 1
7 CONFIGURE LINE 2
21 I0
20 I1
19 I2
18 I3
17 I4
16 I5
15 I6
14 I7
2 CLK/OD LINE 2
3 CLK/OD LINE 1
22 B1
23 B2
24 B3
12 B4
11 B5
10 B6
9 B7
8 B8
1 VCC
25 GND
NOTE: THIS SCHEMATIC TO BE USED WITH 410-1427B AND ALL FUTURE REVISIONS.
DATA I/O
MMI PAL ANALOG
SIZE D
CODE IDENT NO
DRAWING NO 008-1427
SCALE NONE
SHEET 1 OF 1

DATE	SYM	REVISION RECORD	DR.	CK
5-78	A	RELEASE	GJ	GJ
8-78	B	ECN #2383	GB	GB
10-78	C	ECN #2532	GB	GB
11-78	E	ECN #2568	GB	GB



PAL LABEL:

6A-1427E

20-1021-3D

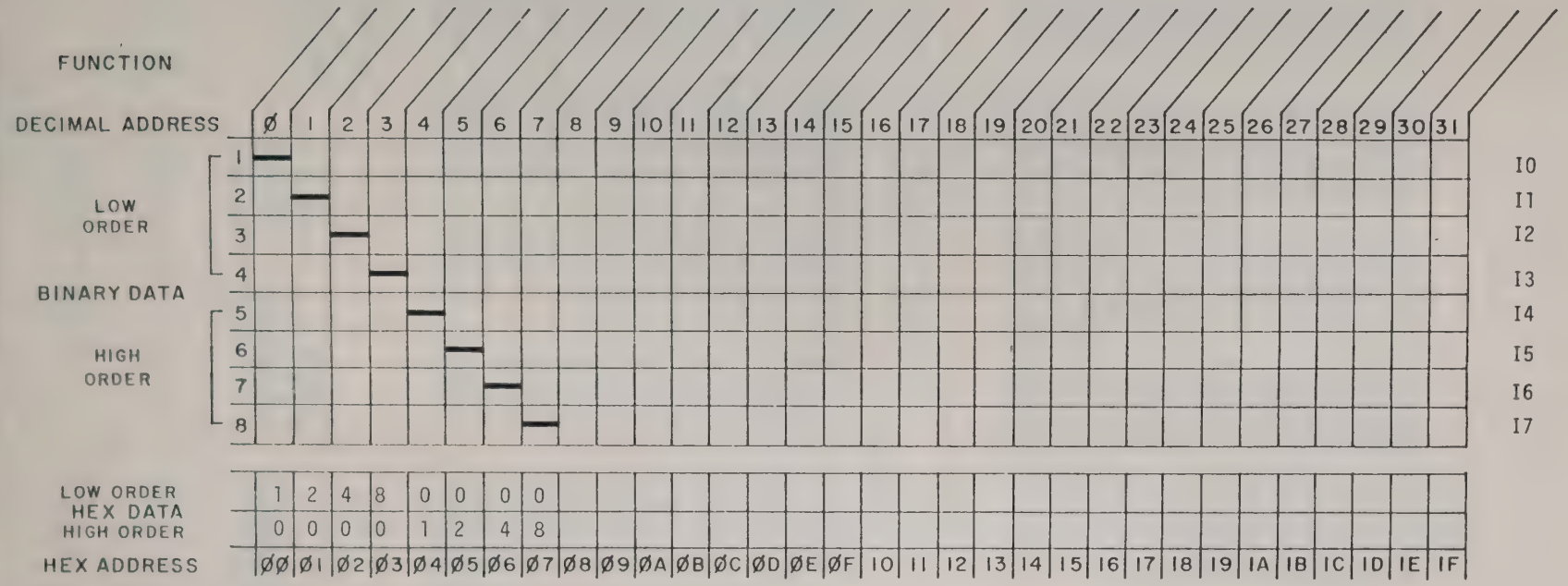
"U" LOCATION

BOARD NUMBER

DASH NUMBER & REV.

TOLERANCES (EXCEPT AS NOTED)	DATA I/O		ISSAQUAH, WASH.
DECIMAL ±	TRUTH TABLE	SCALE	DRAWN BY G.James
			APPROVED BY
FRACTIONAL ±	TITLE M.M.I. PAL U6 (ANALOG)		
ANGULAR ±	DATE 6-8-78	DRAWING NUMBER 010-1427	Sheet 1 of 3

DATE	SYM	REVISION RECORD	DR	CK
		See Sheet 1		


FUNCTION
DECIMAL ADDRESS
Ø 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
LOW ORDER
BINARY DATA
HIGH ORDER
1 2 3 4 5 6 7 8
I0 I1 I2 I3 I4 I5 I6 I7
LOW ORDER HEX DATA HIGH ORDER
1 2 4 8 0 0 0 0
0 0 0 0 1 2 4 8
HEX ADDRESS
ØØ Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8 Ø9 ØA ØB ØC ØD ØE ØF 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F

NOTES

1. LINE = HI (1) = PAPER TAPE HOLE
2. NO LINE = LOW (0) = NO PAPER TAPE HOLE
3. FOR V_{OL} PROGRAMMING PROMS, INVERT SWITCH ON READER DRIVER CARD MUST BE INVERT.

PROM LABEL

13A-1427E

20-1021-3D

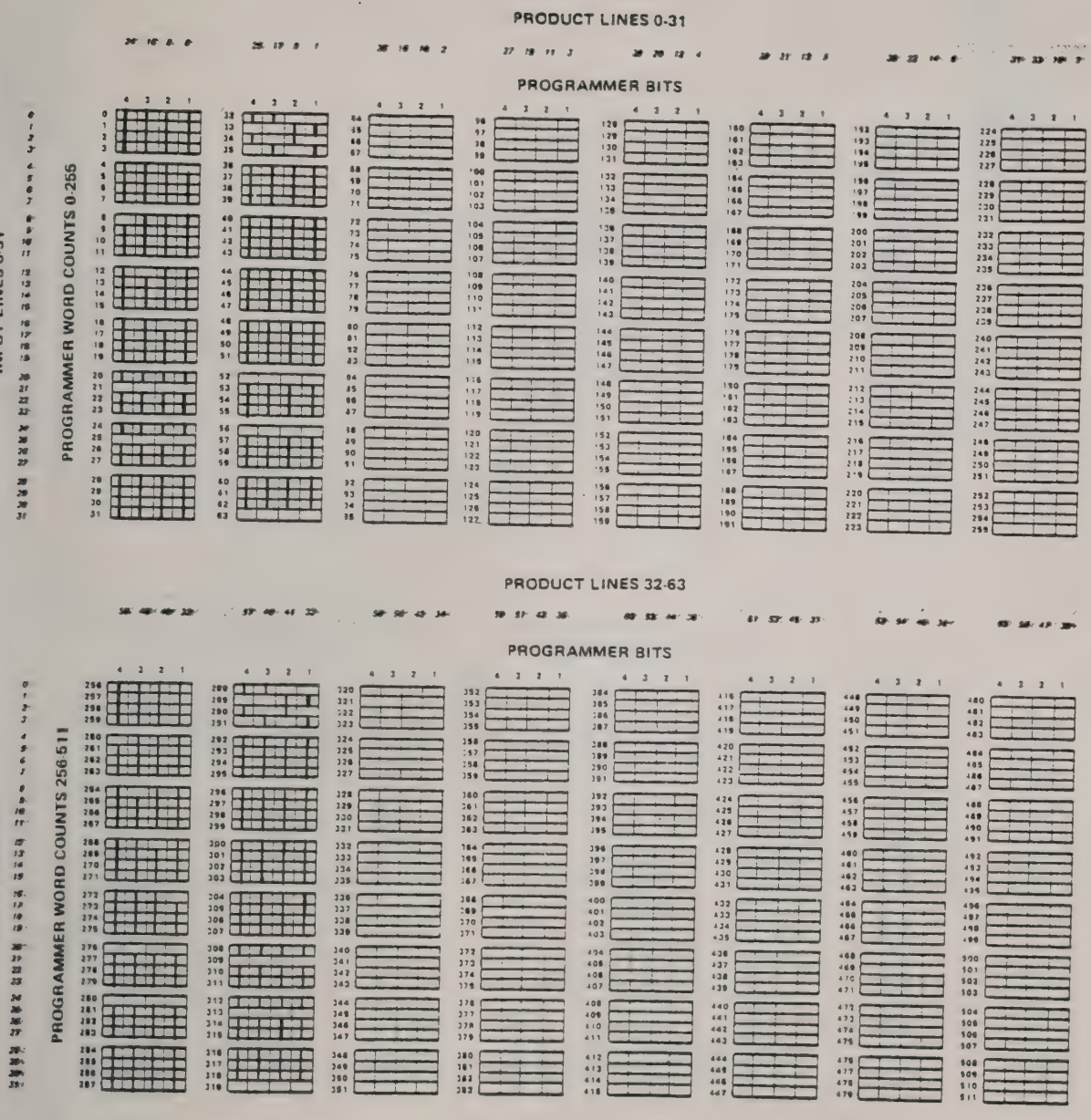
"U" LOCATION

CARD NUMBER

DASH AND REVISION

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL .	M.M.I. PAL	SCALE	DRAWN BY G.J.
FRACTIONAL .	TITLE U13 ADDRESS DECODE (ANALOG)		APPROVED BY
ANGULAR .	DATE 5-30-78	DRAWING NUMBER 010-1427	SHT 2/3

DATE	SYM	REVISION RECORD	DR.	CK
		See Sheet 1		



PAL LABEL:

8A-1427E

20-1021-3D

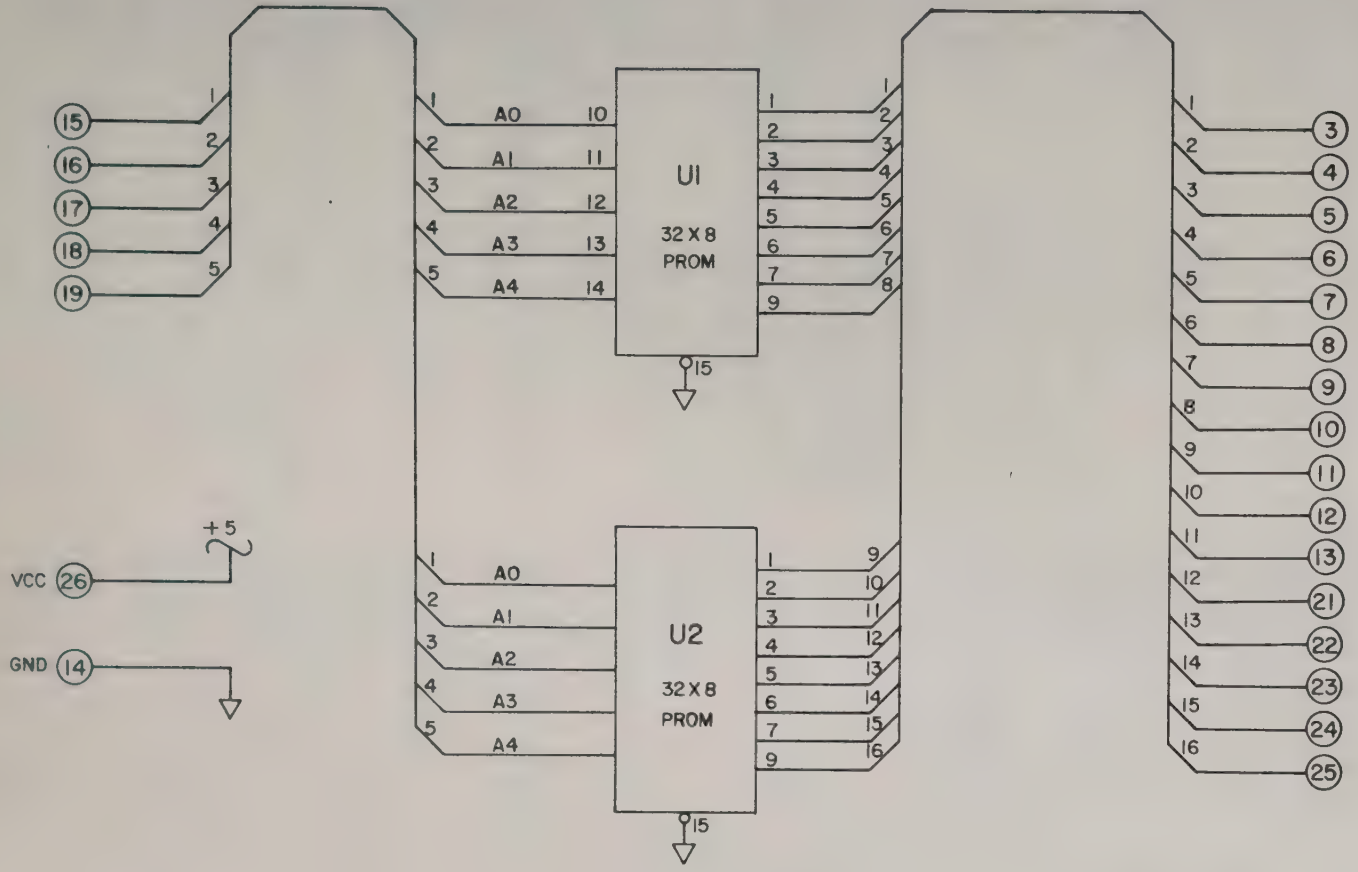
"U" LOCATION

BOARD NUMBER

DASH NUMBER & REV.

TOLERANCES (EXCEPT AS NOTED)	DATA I/O		ISSAQUAH, WASH.
DECIMAL ±	TRUTH TABLE	SCALE	DRAWN BY G. James
			APPROVED BY
FRACTIONAL ±	TITLE M.M.I. PAL U8 (ANALOG)		
ANGULAR ±	DATE 8-8-78	DRAWING NUMBER 010-1427	Sheet 3 of 3

DATE	SYM	REVISION RECORD	DR	CK
11-15-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ±		SCALE	DRAWN BY G. ROPPE
FRACTIONAL ±	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED
ANGULAR ±	DATE 10-15-75	DRAWING NUMBER 008-1072	

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_____

Did you find errors in this manual: _____

How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

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Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ○ ○ NO
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ○ ○ NO
Did the equipment operate on power-up? . . . . . YES ○ ○ NO
Did you attain adequate system performance? . . . . . YES ○ ○ NO
Were any electrical adjustments required? . . . . . YES ○ ○ NO
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ○ ○ NO

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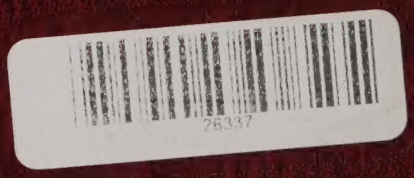

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